Electronics for HL-LHC

Challenges and Outlook

Ph. Farthouat

CERN

TWEPP-14 / Aix-en-Provence

Thanks and Disclaimer

- I'd like to thank my colleagues from ATLAS and CMS who provided most of the material presented
  - References and ackowledgements on the last slide
- Only the front-end electronics will be presented
  - Because of lack of time
  - Despite the very challenging electronics systems to be developped for the back-end electronics (in particular for the track trigger)
- All presented material is valid today or has been valid until last month
- It might not be valid at the start of HL-LHC

Outline

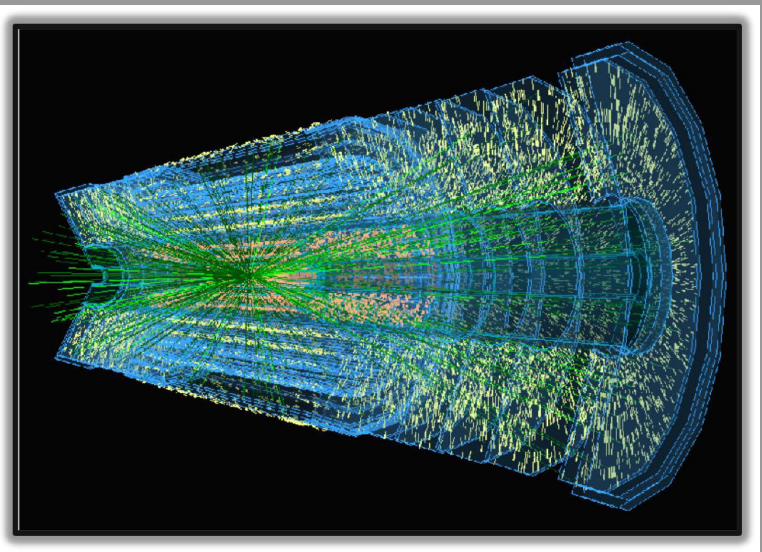
Outline

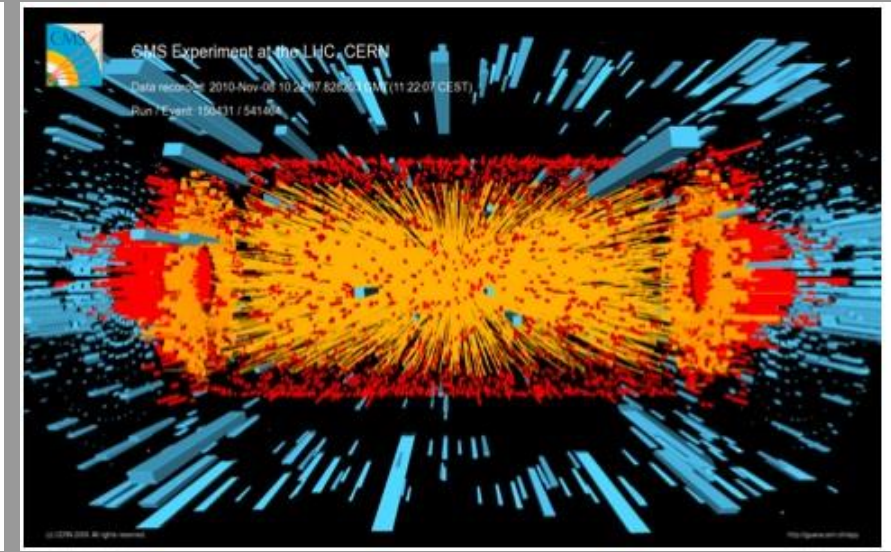
LHC and HL-LHC Schedule

- Main points:
  - Luminosity increase
  - Physics for HL-LHC to start in September 2025
  - 11 years from now

Main differences between LHC and HL-LHC
With impact on the readout electronics

	LHC	HL-LHC
Instantaneous luminosity [$cm^{-2}.s^{-1}$]	10^{34}	$5\ 10^{34}$
Number of events per BC at 25 *ns*	28	140
Number of events per BC at 50 *ns*	56	280
Integrated luminosity [fb^{-1}]	300	3000





Outline

Impact on Radiation Hardness Requirements

For Electronics

- Radiation constraints at LHC: 10 years ($10^8 s$) at 10^{34} i.e. 1000 fb^{-1}
- HL-LHC: 3000 fb^{-1} i.e. 3 times more radiation (TID and NIEL)
- Electronics qualification for LHC
  - Large safety factor on the simulated values
- Safety factors can be reduced for LH-HLC
  - Good agreement simulation vs measurement

ATLAS safety factors for LHC and HL-LHC

	Tracker	Elsewhere
TID	1.5 / 1.5	3.5 / 1.5
NIEL	5 / 1.5	5 / 2
ratio HL-LHC/LHC for TID	3	1.3
ratio HL-LHC/LHC for NIEL	0.9	1.2

Impact on Radiation Hardness Requirements

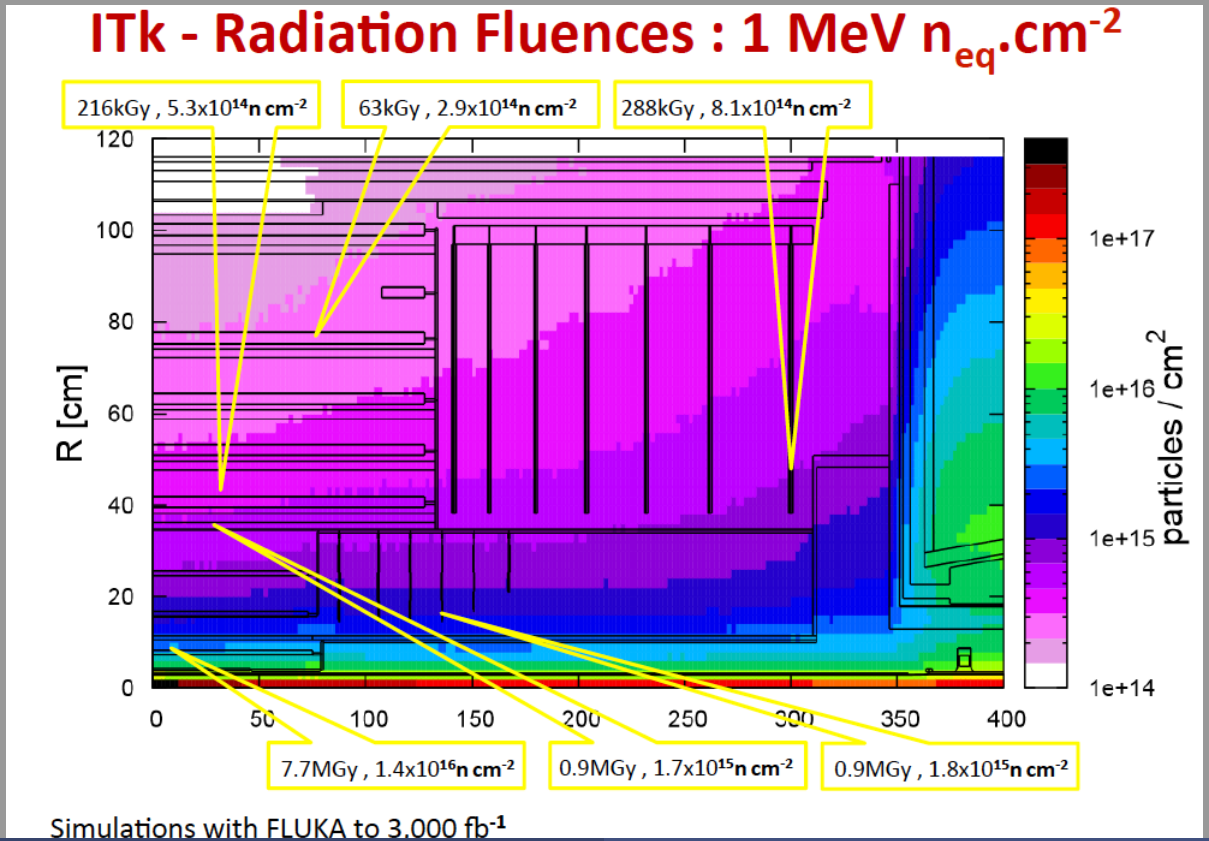
Outside Tracker

Small increase (20–30%) of radiation constraints

Tracker

≈ 10 *MGy*

$\approx 10^{16}$ $1MeV.n.cm^{-2}$



Outline

Impact on Event Size
High Event Multiplicity

New tracker for both ATLAS and CMS

Higher granularity

- e.g. silicon strips 2.5 and 5 *cm* vs O(10 *cm*)

Higher number of channels

- e.g. in CMS outer tracker O(250 *Mch*) vs 9.3 *Mch*

And occupancy per channel similar to current one

Rest of the detector (almost) unchanged

But higher occupancy leads to higher event size

Event size O(5 *MB*) vs 1–2 *MB*

Impact on Trigger Rate

Current L1 trigger in ATLAS and CMS based on calorimeters and muon spectrometers only

- 100 *kHz* rate
- 2.5/3.2 μs latency (ATLAS/CMS)

Maintaining current physics sensitivity at HL-LHC very challenging for the trigger

- Cannot increase p_T threshold
- Background from pileup reduces capabilities
  - Isolation more difficult
  - Jet p_T and missing E_T impacted

Expected Trigger Rates

Trigger improvements for HL-LHC

- Using higher granularity for calorimeter trigger
- Using muon precision chambers to improve p_T cuts
- Using tracking information

ATLAS

- L0 (calorimeter and muon)
  - 1*MHz* and 6–10 μs
- L1 including tracking
  - 400 *kHz* and 30–60 μs

CMS

- L1 (calorimeter, muon and tracking)
  - 1 *MHz* and 10 μs

High radiation in the trackers

- Up to 10 *MGy* and 2 10^{16} $1MeV.n.cm^2$

Large event size

- Order of 5 *MB*

High trigger rate

- Up to 1 *MHz*

Large amount of data to handle

- Up to 5 $PB.s^{-1}$

Common challenges for the electronics of ATLAS and CMS

- Radiation hard IC technology
- High speed links
- Low power design and efficient power distribution

Outline

New Trackers for ATLAS and CMS

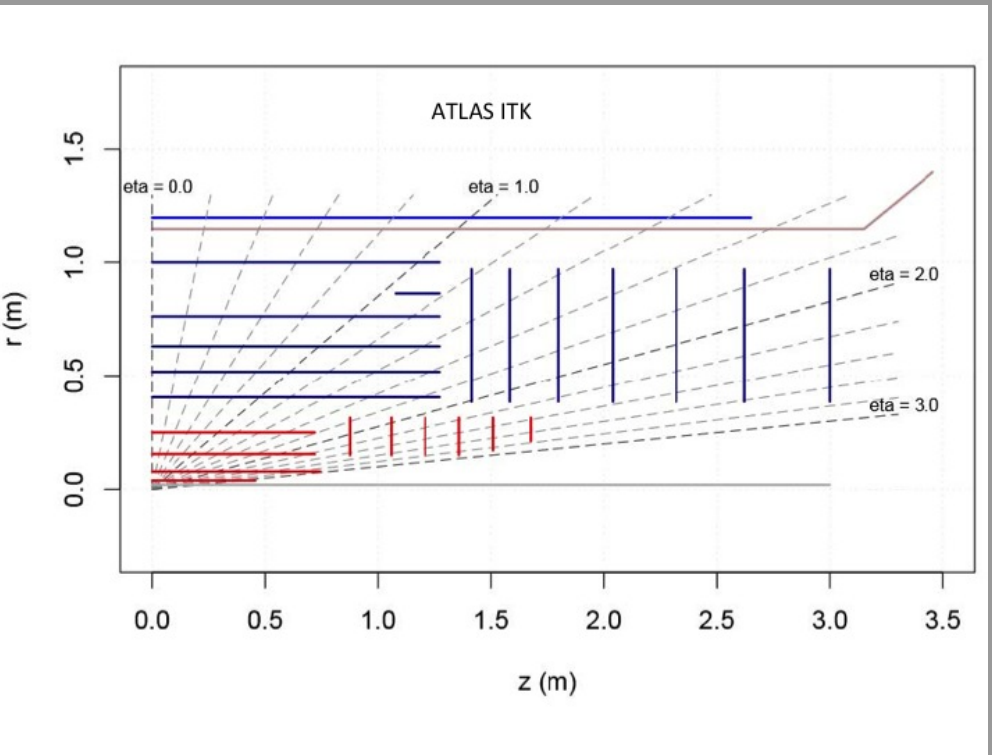
ATLAS

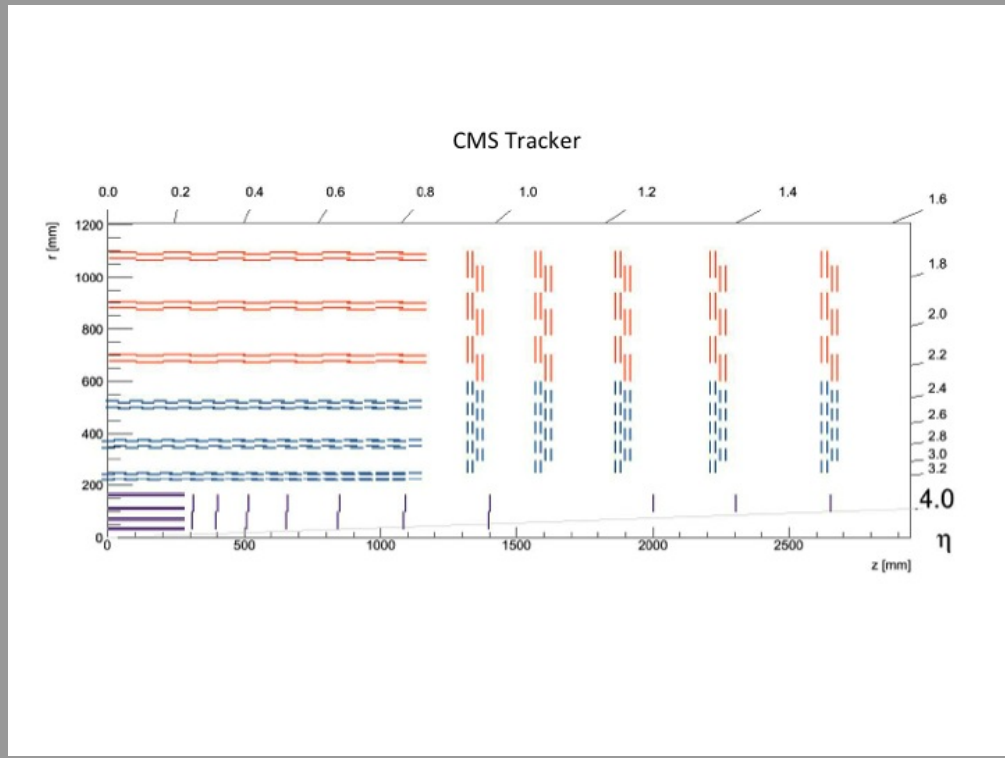
- Silicon tracker
- Pixel detector
  - 4 barrel layers
  - 6 end-cap disks
  - pixel size 25 x 100 μm^2
  - 8.2 m^2 / 638 *Mch*
- Strip detector
  - 5 and 2.5 *cm* strips
  - 5(+ 1 stub) barrel layers
  - 7 end-cap disks
  - 193 m^2 / 74 *Mch*

CMS

- Silicon tracker
- Pixel detector
  - 4 barrel layers
  - up to 10 end-cap disks
  - pixel size
    50 x 50 or 25 x 100 μm^2
  - 4 m^2 / O(1 *Gch*)
- Outer tracker
  - 6 barrel layers
  - 7 end-cap disks
  - Strips and pixels-strips
  - 210 m^2 / 250 *Mch*

Trackers Layouts





Outline

Main Challenges

Environment

- High radiation levels. Up to 1 *Grad* & 2 10^{16} $1MeV.n.cm^2$
- Extreme particle flux
  - From 200 $MHz.cm^{-2}$ in the current system to 2 $GHz.cm^{-2}$
  - 50 *kHz* per pixel for a 50 x 50 μm^2 pixel

Data rate

- Data rate 22 $Gb.s^{-1}.cm^{-2}$ for a triggerless system
  - 1800 $Tb.s^{-1}$ for 8 m^2 !!
- Still 220 – 550 $Mb.s^{-1}.cm^{-2}$ for a 0.4 – 1 *MHz* readout rate

ATLAS-CMS common effort

RD53 collaboration

RD53: ATLAS – CMS Collaboration

- About 20 institutes and 100 collaborators (50% chip designers)
- 6 Working Groups
  - WG1: Radiation tests and qualification
  - WG2: Top level
  - WG3: Simulation/verification framework
  - WG4: I/O
  - WG5: Analog front-end design
  - WG6: IP blocks
- RD53 web site: www.cern.ch/RD53/

Design of a prototype chip in 65 *nm* technology
Availability in 2016

RD53 Critical Issues

Establish guidelines for radiation hardness of the selected 65 *nm* technology to 1 *Grad*

- Or decide the process cannot be used to this level

Develop tools and methodology adequate for $5x10^8$ transistors mixed signal chip in this technology

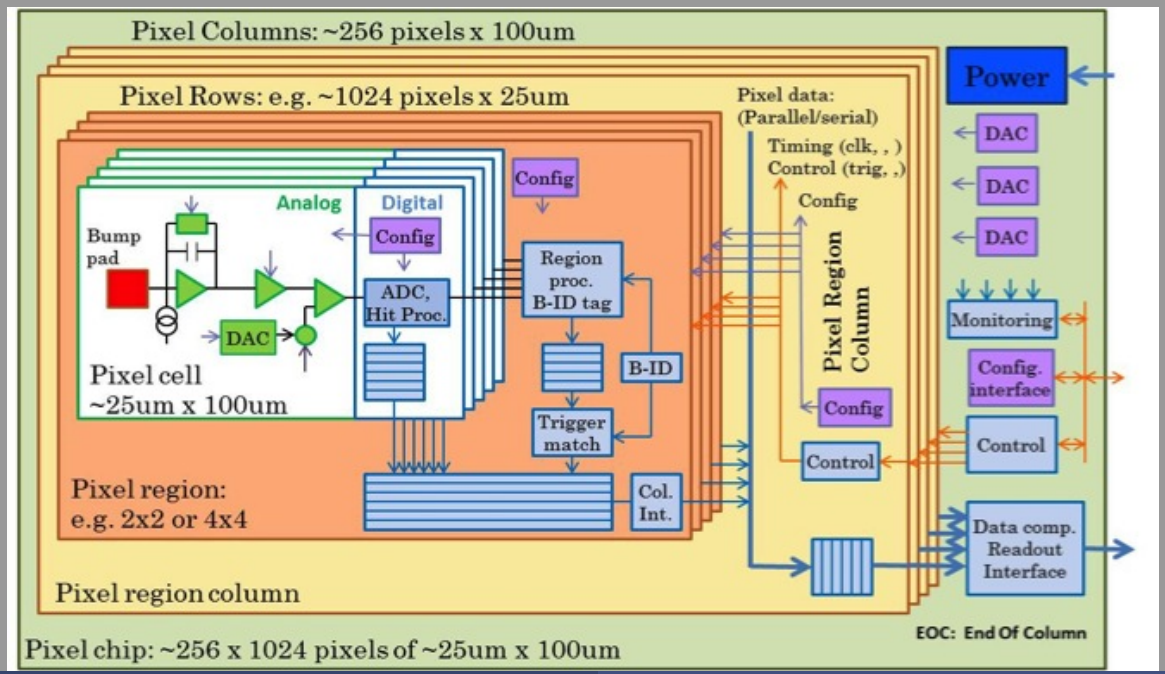
Define pixel size and low threshold operation strategy

- 50 x 50 μm^2 chip pixels (sensor aspect ratio can vary)

Develop high bandwidth readout ($2 - 4$ $Gb.s^{-1}$ / chip) including cable transmission models

Chip Architecture

- Pixel 50 x 50 or 25 x 100 μm^2
- 256 *kchannels* per chip
- Trigger latency O(10 μs)
- Trigger rate up to 2 *MHz*
- Charge digitization (ToT or ADC)
- Buffering within the pixel region
- Data compression at the end of column
- 95% digital chip (as FEI4)
- Output links @ 1 – 4 $Gb.s^{-}1$



Readout Links

Optical devices not radiation hard enough to be installed close to the pixel chips

- Need for a few meters electrical transmission
- Need very low mass cables

One chip handles 256 *kchannels* and covers O(6 cm^2)

- Readout bandwidth 1 – 4 $Gb.s^{-1}$
- Aim at electrical links @ 1.2 $Gb.s^{-1}$

Some measurements

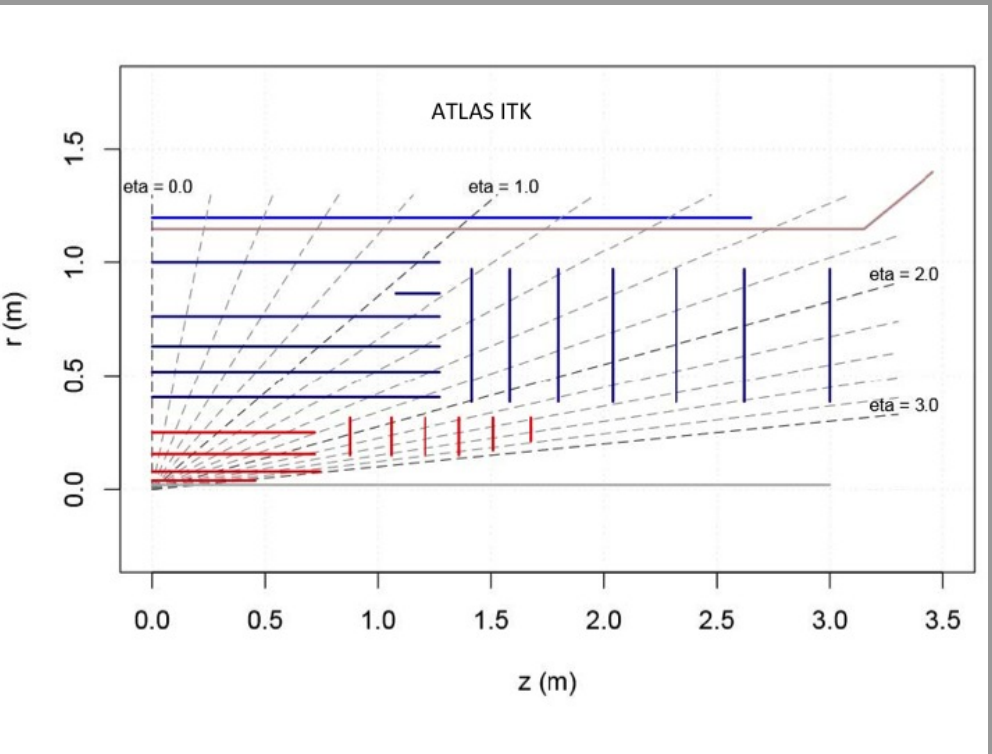
- Twinax cables 4 – 6 $Gb.s^{-1}$ over 4 m
- PSI very low mass twisted pair: 400 $Mb.s^{-1}$ over 1 m

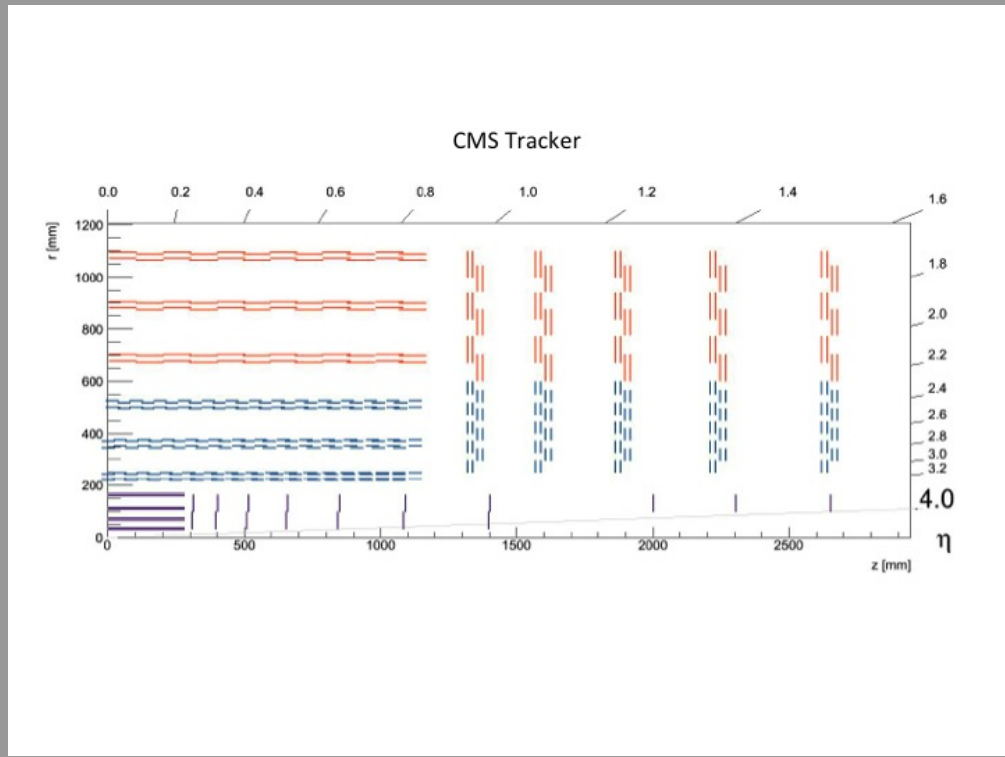
Pixel ASIC Generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2: HL-LHC
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	**~ 50x50um^2**
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, HVCMOS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20 mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	**~1G**
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**1-2 GHz/cm^2**
Trigger rate	100kHz	100KHz	200kHz - **1MHz**
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 - **20us**
Hit memory per chip	0.1Mb	1Mb	~16Mb **(160x)**
Readout rate	40Mb/s	320Mb/s	**1-4Gb/s (100x)**
Radiation	**100Mrad**	**200Mrad**	**1Grad**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	**Digital**
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	**In Pixel buffering**
Power	~1/4 W/cm^2	~1/4 W/cm^2	**1/2 - 1 W/cm^2**

Outline

Trackers Layouts





Main Challenges

Environment

- Radiation level up to O(100) *Mrad* & 10^{15} $1MeV.n.cm^2$

Data rate

- Data rate O(10 $Tb.s^{-1}$)
  - Readout @ L1 (or L0) rate
  - Outer tracker part of the L1 trigger. Trigger data:
    - @ 40 *MHz* for a self seeded trigger
    - @ L0 rate for a region of interest (RoI) based trigger

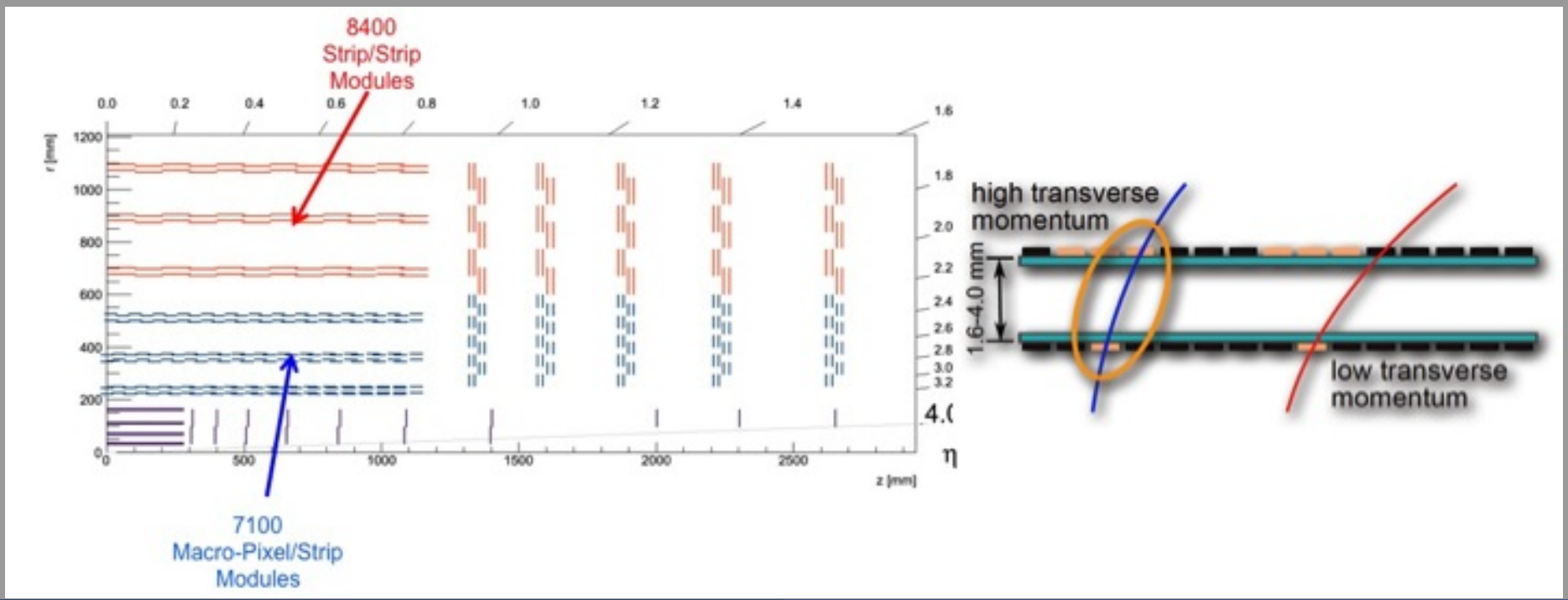
Large differences between ATLAS and CMS

- Mainly for the trigger part

CMS Outer Tracker

Two types of modules

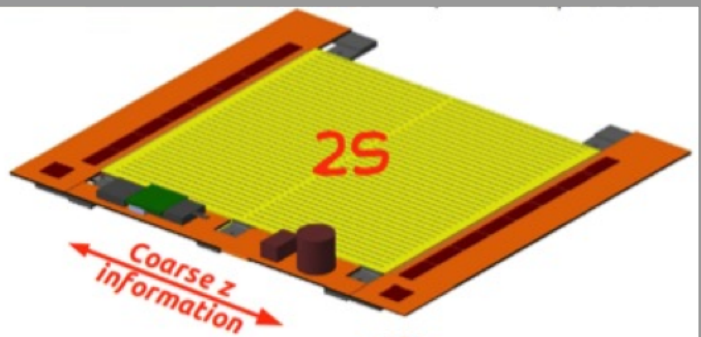
- Strip/Strip modules
- Macro-Pixel/Strip modules
- Both participating in the trigger



CMS Outer Tracker Modules

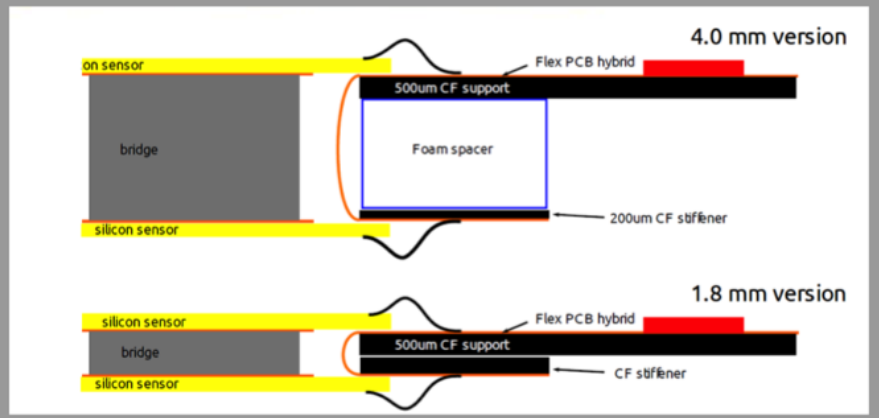
Each module is an independant block with its own services

2 Strip sensors
Strips: 5 cm × 90 µm
Strips: 5 cm × 90 µm
P = 2.7 W
~ 92 cm² active area
For r > 40 cm

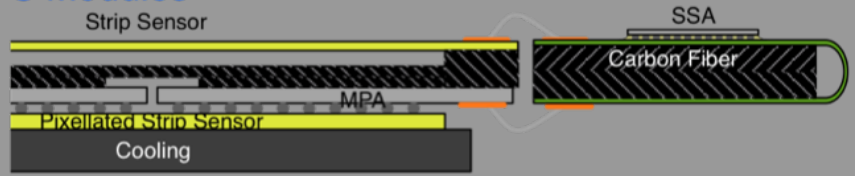


Pixel + Strip sensors
Strips: 2.5 cm × 100 µm
Pixels: 1.5 mm × 100 µm
P = 5.0 W
~ 44 cm² active area
For r > 20 cm

2S Modules

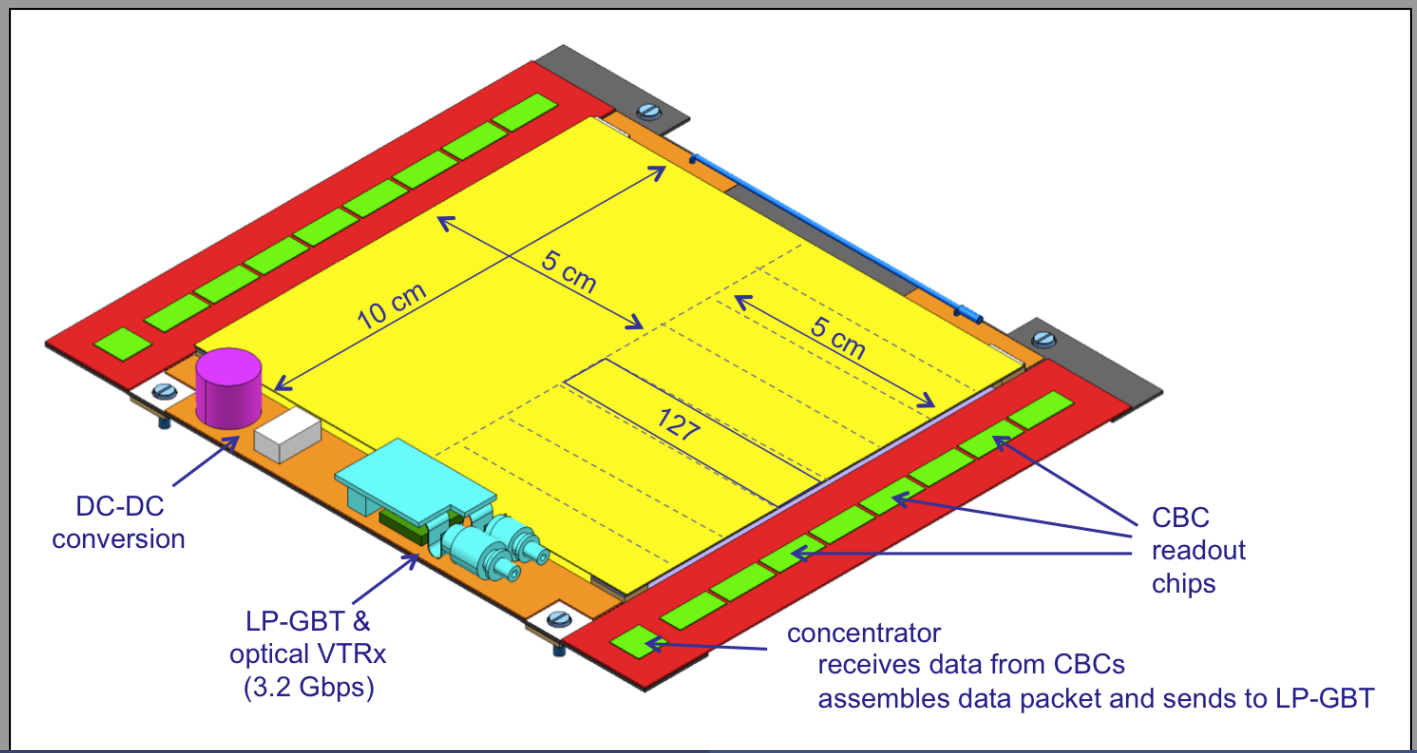


PS Modules

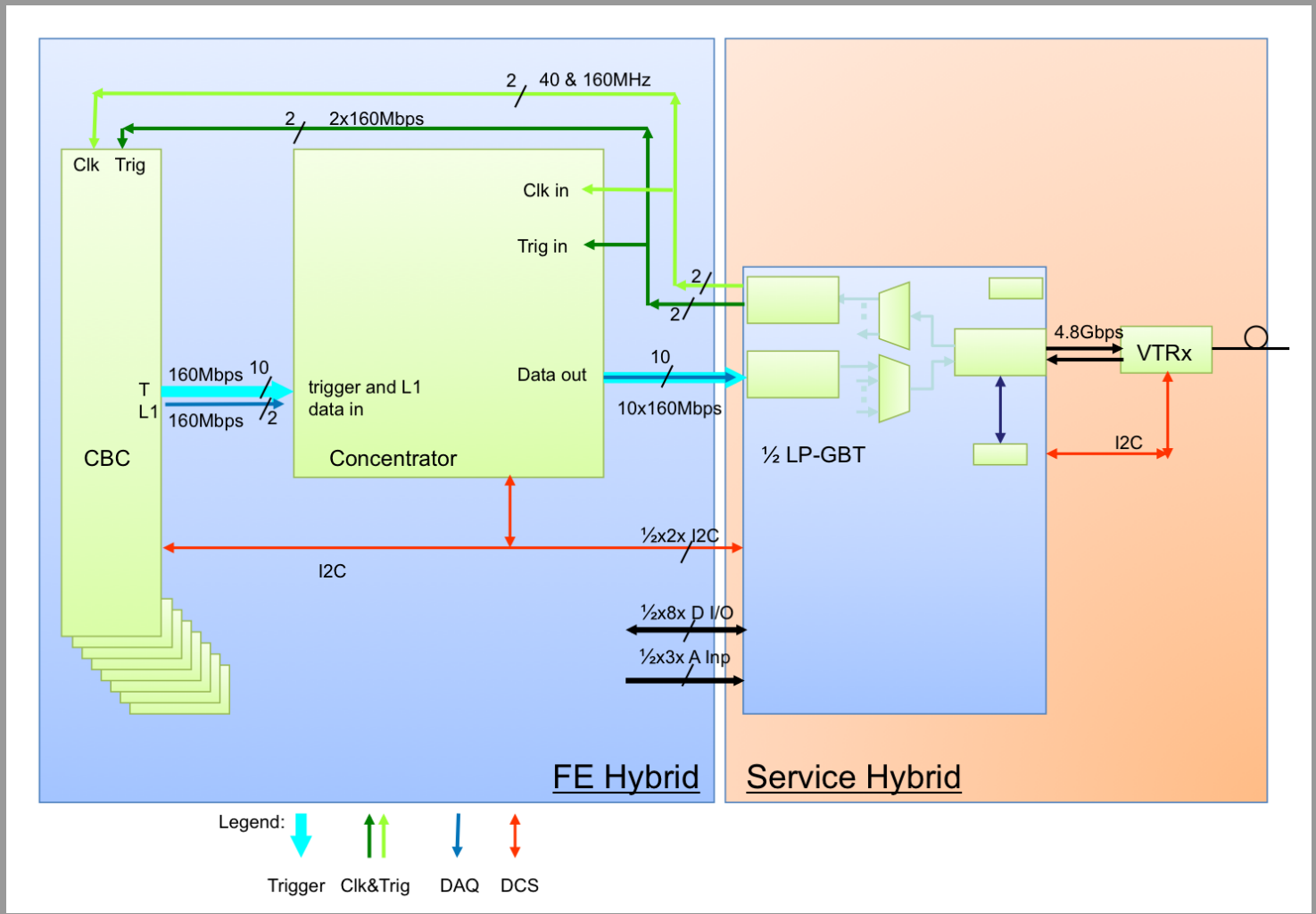


CMS 2S Modules

- 254-ch readout chip: CBC
- Concentrator ASIC
- 130 *nm* CMOS technology
- C4 technology (no bonding)
  - High density hybrid required



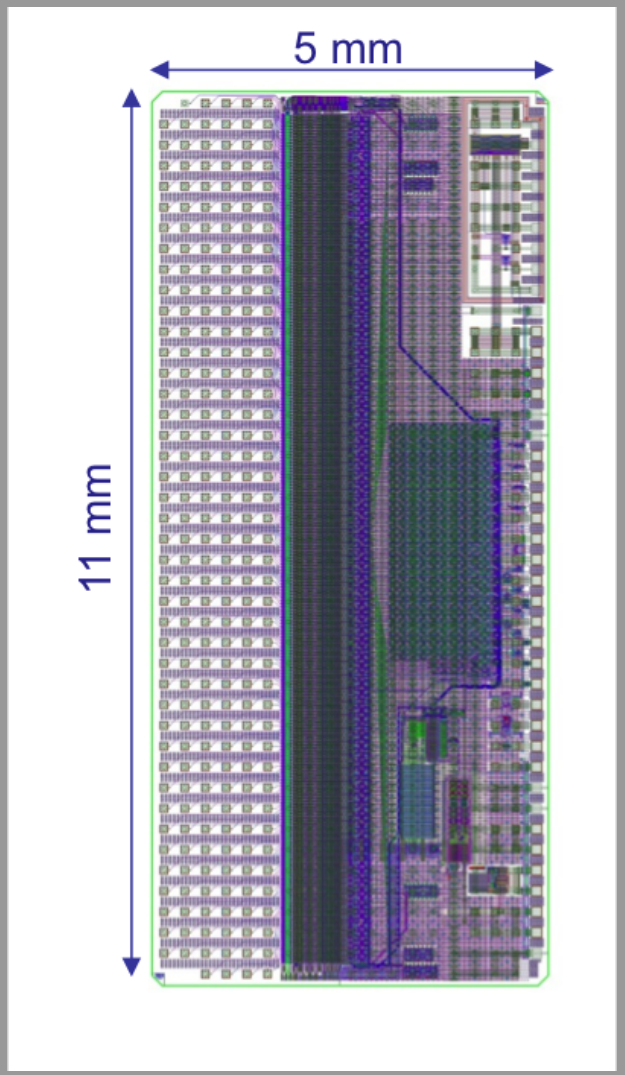
Simplified Block Diagram



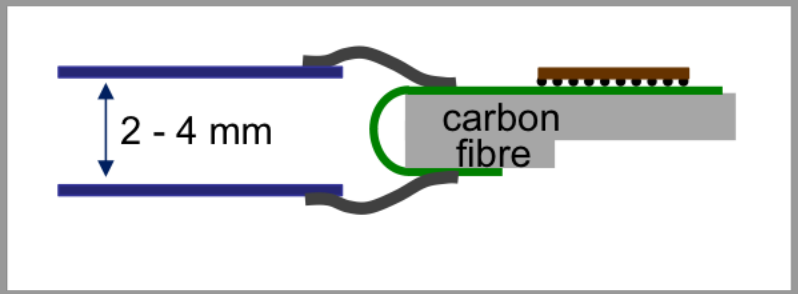
3.2 $Gb.s^{-1}$ per module

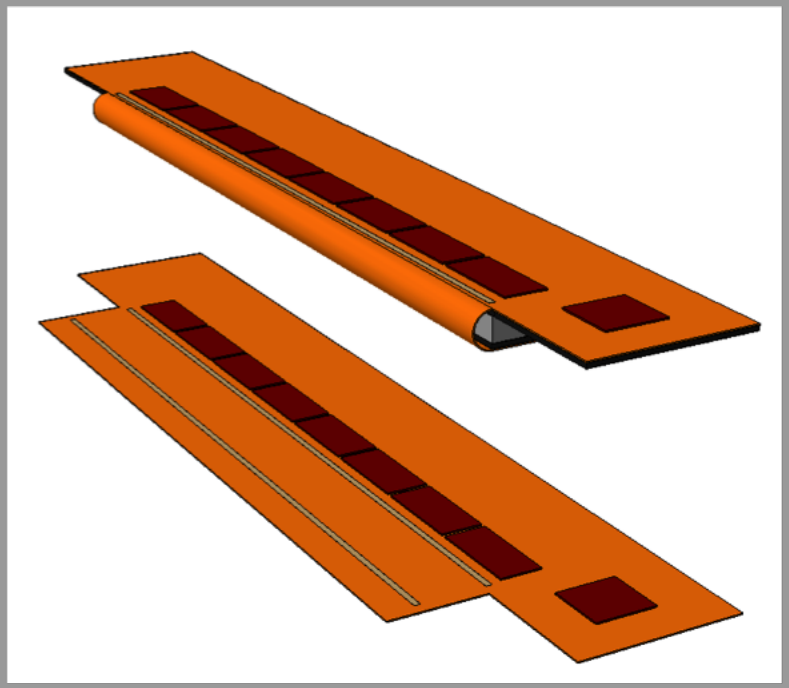
CMS CBC ASIC

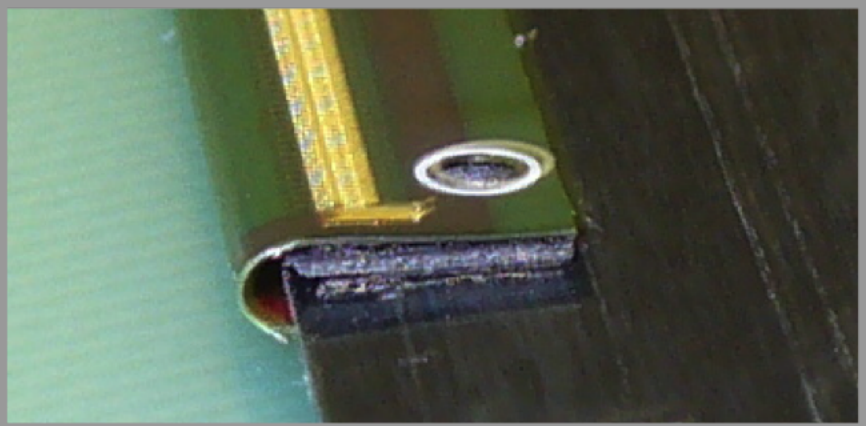
- 254 channels in 130 *nm* CMOS
- Front end designed for up to 5 *cm* strips
  - 1000 e^- *rms* noise
- DC coupled, both sensor polarities
- Binary unsparsified readout
- Pipeline length 6.4 μs
- Bump-bond layout
  - C4 bump-bond layout, 250 μm pitch
  - 19 columns x 43 rows
- Includes triggering features
  - 30 interchip signals (15 in, 15 out)
  - top and bottom
- 350 μW per channel

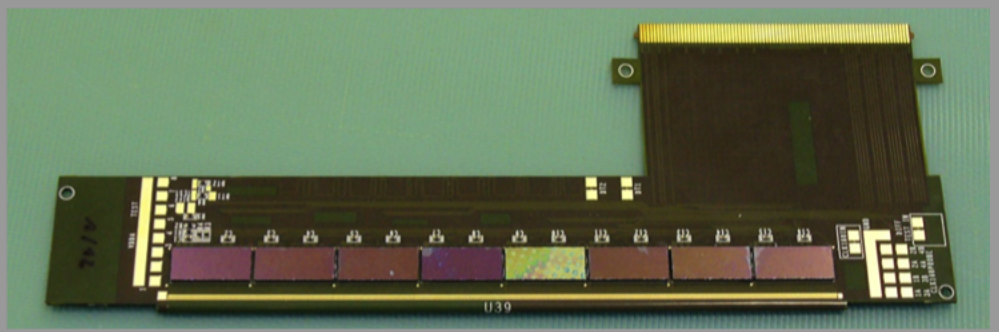


CMS 2S Hybrid Development



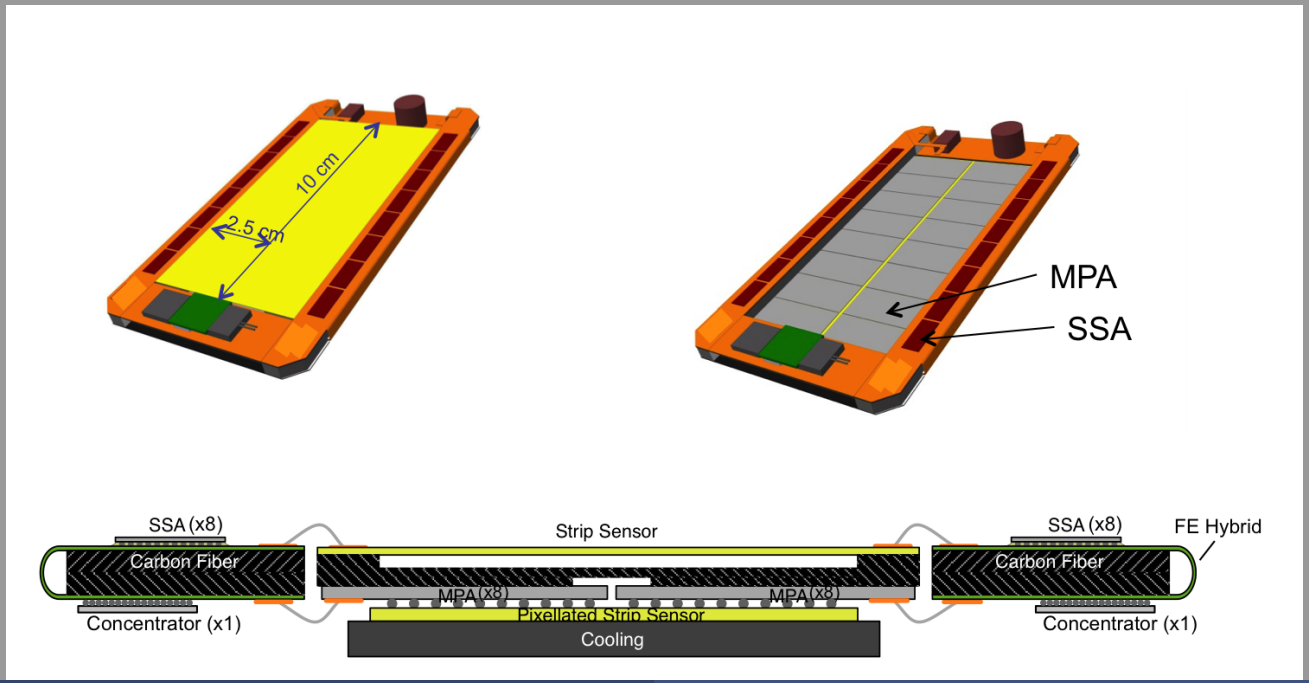






CMS PS Modules

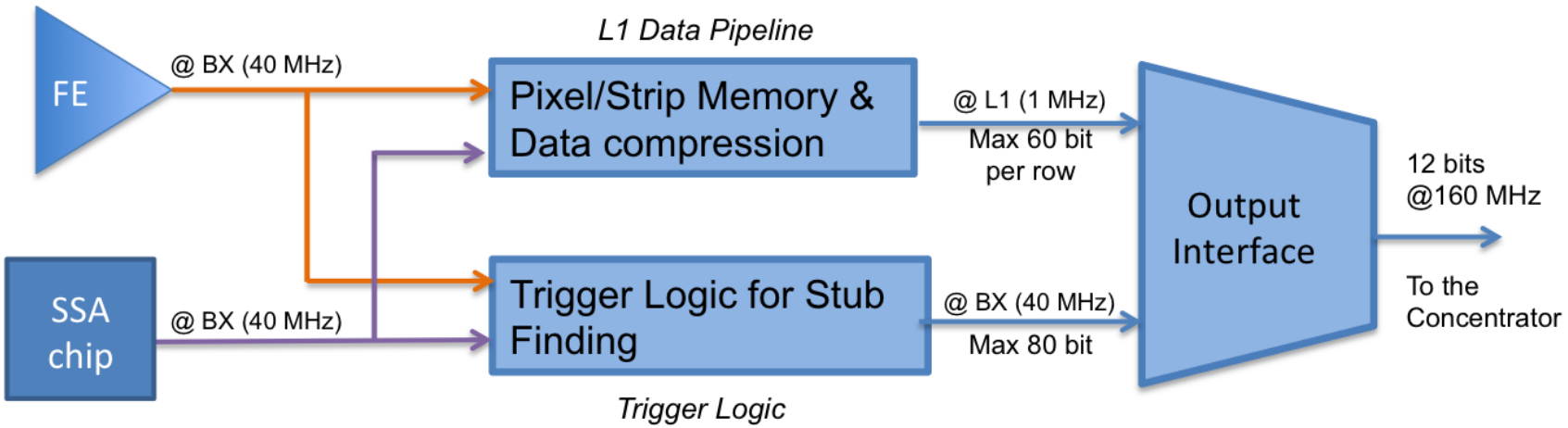
- 3 ASICs in 65 *nm* CMOS
  - SSA, MPA & Concentrator
- 120 strips per SSA
  - 100 μm strip pitch
- 120 strips and 16 x 120 pixels per MPA
  - Pixel size: 100 x 1446 μm^2



MPA Readout Data Flow

Input each 25 ns (40 MHz):

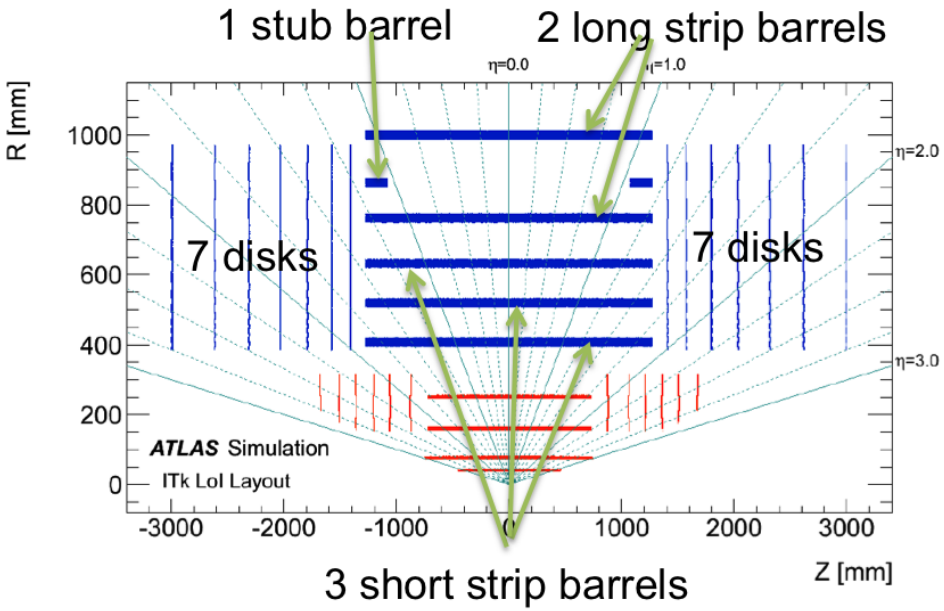
- Pixel hits from Front- End: 120 columns x 16 rows = 1920 hits
- Strip hits from SSA chip: 120 hits



ATLAS Outer Tracker

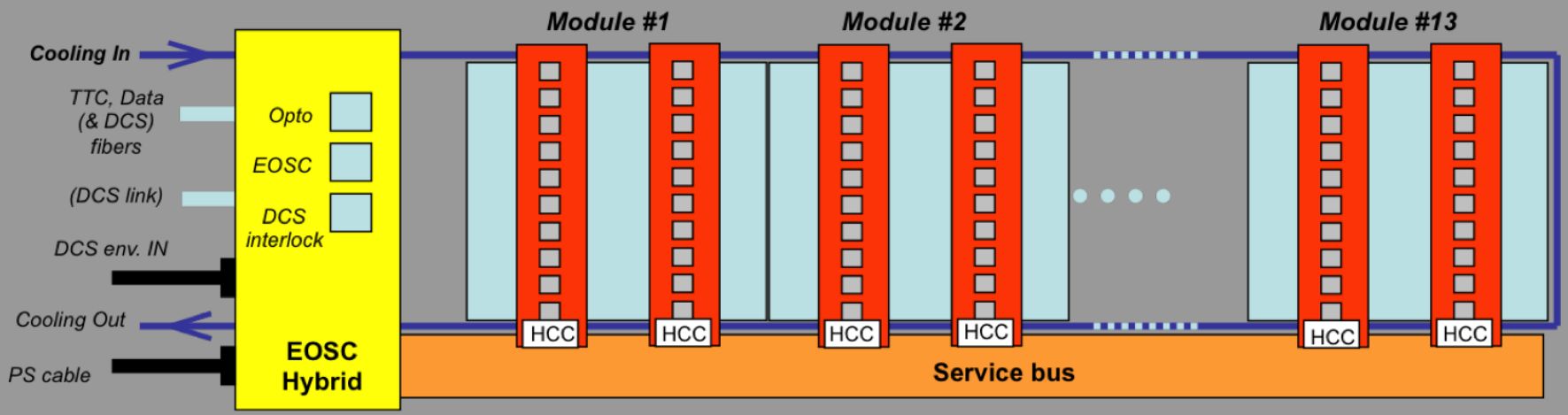
Two types of modules

- Short strip modules
- Long strip modules
- Organised in double-sided staves with stereo angle



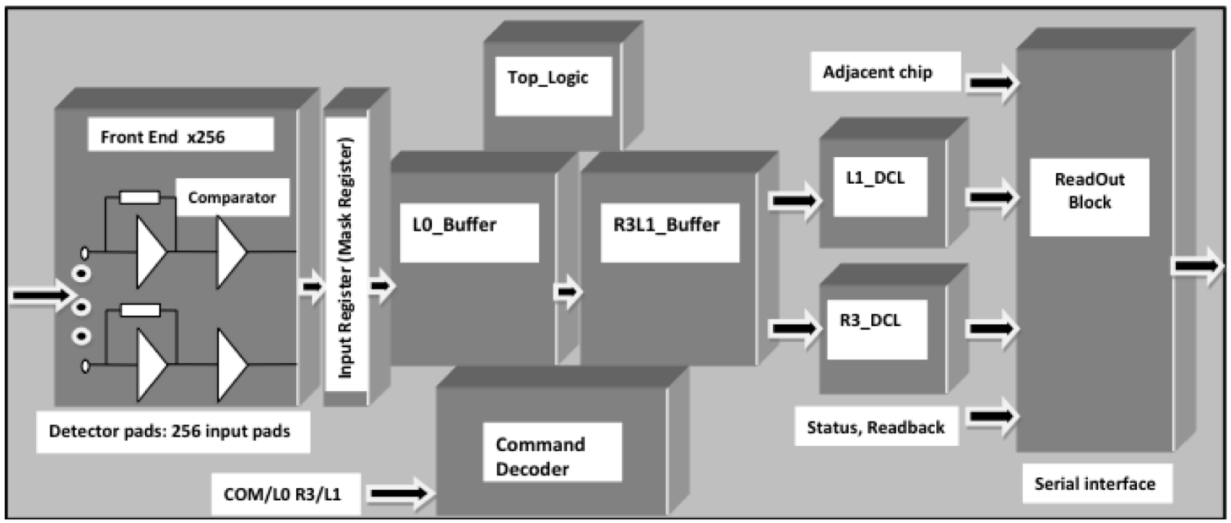
ATLAS Stave Readout

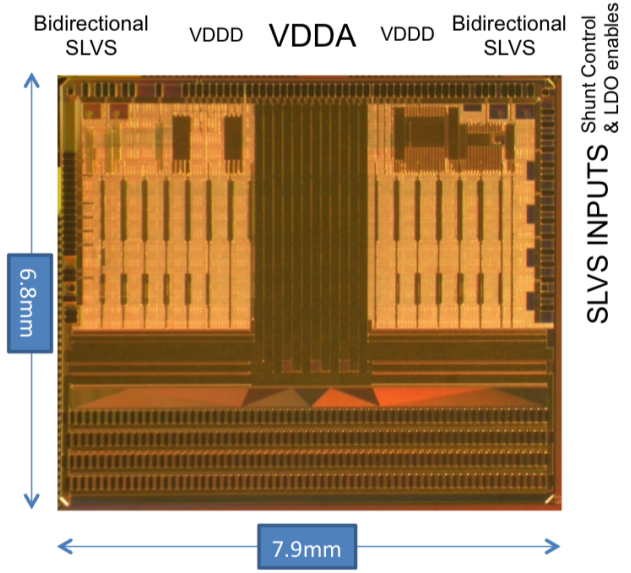
- Two ASICs in 130 *nm* CMOS
  - ABC130 and HCC
- Region of Interest concept
  - L0 (400 *kHz*) delivers region of interest
  - About 10% of the tracker data to be readout for L1 decision
  - L1 (200 *kHz*) used for complete readout
- Buffers in the front-end
  - L0 pipeline (6.4 μs)
  - L1 buffer storing up to 256 events after L0 until L1
- Serial links (e-link) between the HCC's and the End of Stave GBT
  - 160 $Mb.s^{-1}$ HCC to EOS
  - 4.2 $Gb.s^{-1}$ for the stave



ABC130

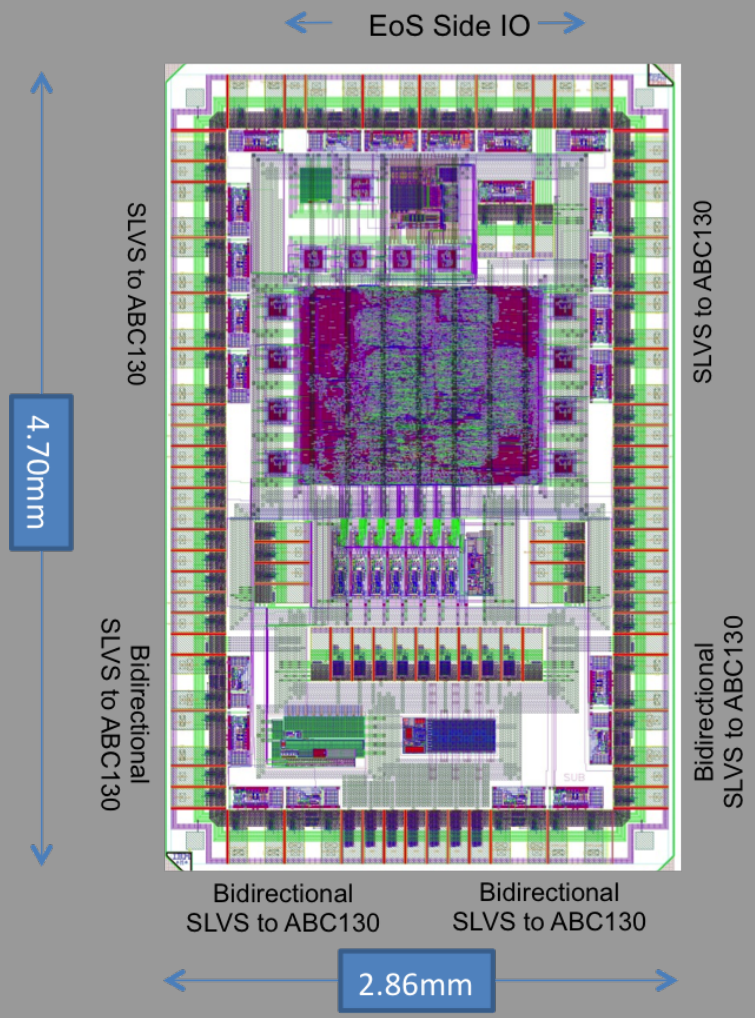
- 256-channel 130 *nm* CMOS
- Pad frame optimized for hybrid mass reduction
  - Direct sensor bonding
  - All power bonds at back edge
- Support Serial Powering
- 2-level trigger architecture
  - L0 (400 *kHz*) - L1 (200 *kHz*)
  - Data retrieved from buffer using L0ID tag
- Programmable LDOs for analogue / digital power





Hybrid Controller Chip (HCC)

- 130 *nm* CMOS
- Interfaces between the ABC130s and the EOS card via the stave bus cable
  - SLVS @ 160 $Mb.s^{-1}$
- Programmable delays to time the ABC130
- Prioritization between RoI and readout data



Next Steps for the ATLAS Tracker

Current version

- Designed for L0 @ 400 *kHz*, L1 @ 200 *kHz* and 10% of modules to be part of RoI
- Equivallent to a full readout @ 250 *kHz*

New requirements

- New trigger rates: L0 @ 1 *MHz*, L1 @ 400 *kHz* and 10% of modules to be part of RoI
- Equivallent to a full readout @ 500 *kHz*

Possibility to fully read out at 1 *MHz* L0 being looked at

Upgrades of the Calorimeters and Muon Detectors

No full detector replacement as for the trackers

- Two exceptions:
  - New muon chambers in the end-caps
    - μmegas and sTGC for ATLAS
    - GEM for CMS
  - New CMS end-cap calorimeter

Replacement of most of the readout electronics

- Except for some muon chambers

Outline

Upgrade of the Calorimeters Readout Electronics

Optimisation of the front-end for high pile-up

VFE of CMS Barrel Ecal
ATLAS LAr and Tile calorimeters preamplifier-shaper
ASICs in 130 *nm* CMOS and in SiGe

Readout @ 40 *MHz*

Availability of the complete data in the back-end electronics
Simplification of the front-end architecture
Opens some possibilities for future trigger algorithms

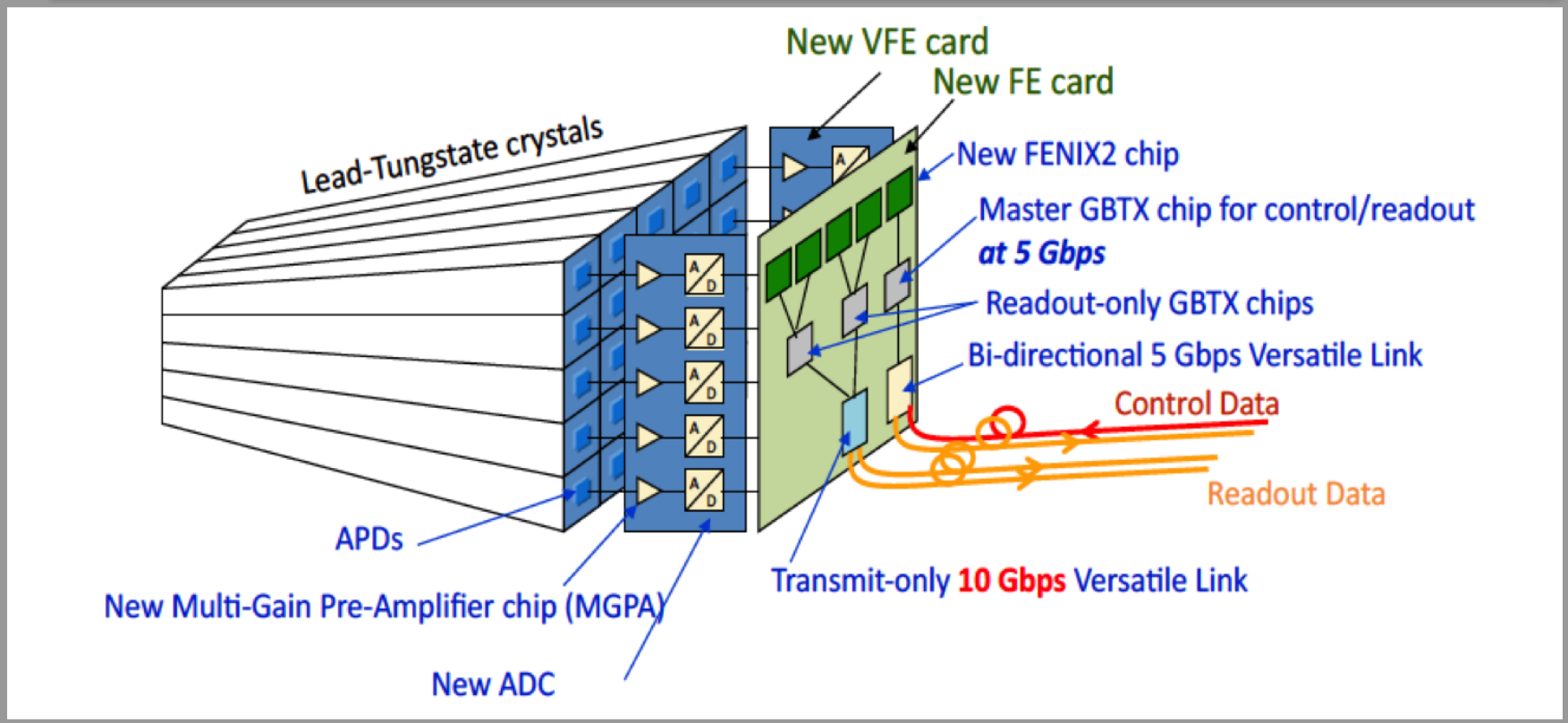
Need for a low power 16-bit – 11-bit ENOB ADC per channel

Need for very high bandwidth links

CMS ECAL Barrel Upgrade

Module readout

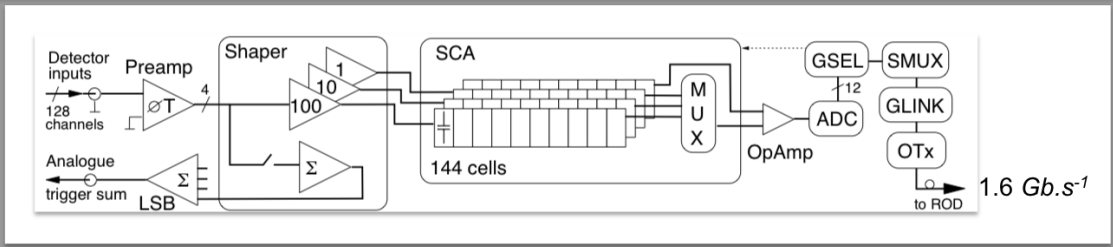
3 readout links @ 5 $Gb.s^{-1}$ to be compared to
2 links @ 800 $Mb.s^{-1}$ in the current system



ATLAS LAr Calorimeter Upgrade

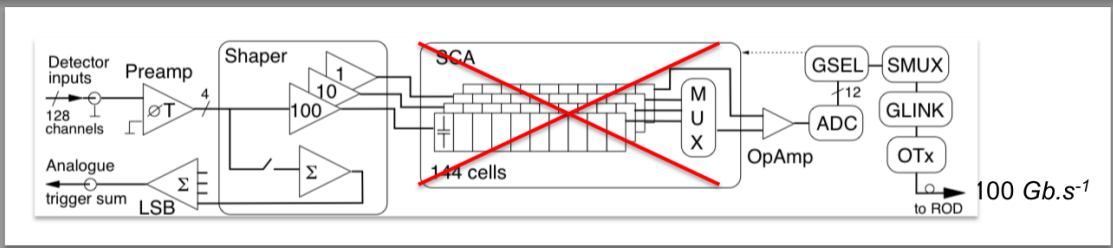
Current front-end board

Analog to digital conversion of the 128 channels after L1
1 readout link @ 1.6 $Gb.s^{-1}$ per FEB



Upgraded front-end board

Analog to digital conversion of the 128 channels @ 40 *MHz*
O(100 $Gb.s^{-1}$) per FEB



Developments for the Calorimeters

Amplifiers-Shapers

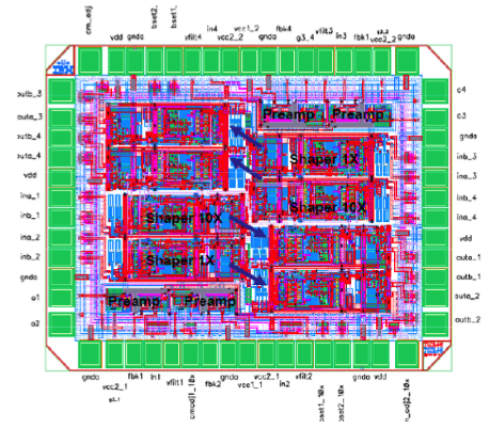
In 130 *nm* CMOS for the ATLAS Tile
Two SiGe versions for the ATLAS LAr

ADCs

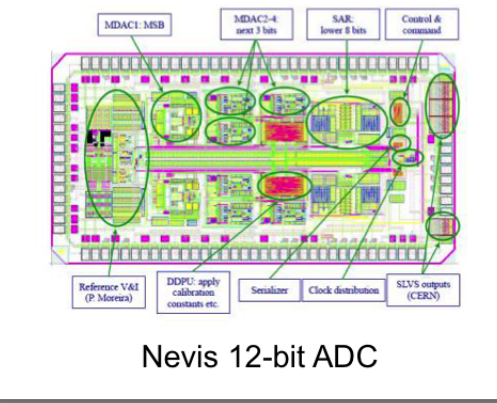
Several 12-bit 40 *MHz* ADC for the ATLAS Tile and LAr (130 *nm* CMOS)
Assuming a readout based on a multigain shaper

Serialisers and Links

Alternatives to the GBT and the Versatile Links being studied
Including optical modulators



LAr Preamp-Shaper



Nevis 12-bit ADC

Possible (Highly Desirable) Common Developments

Very similar requirements for the calorimeters

Preamplifier-Shaper specific to each type
ADC, serialisers and links could be the same

Possible common developments

IP block for a 16-bit, 11–12 ENOB, 40 *MHz* ADC
IP block for a fast serialiser
IP block for a laser driver

Special ASIC for each calorimeter

Integrating a number of the previous blocks

CMS End-Cap High Granularity Calorimeter

Electromagnetic Calorimeter

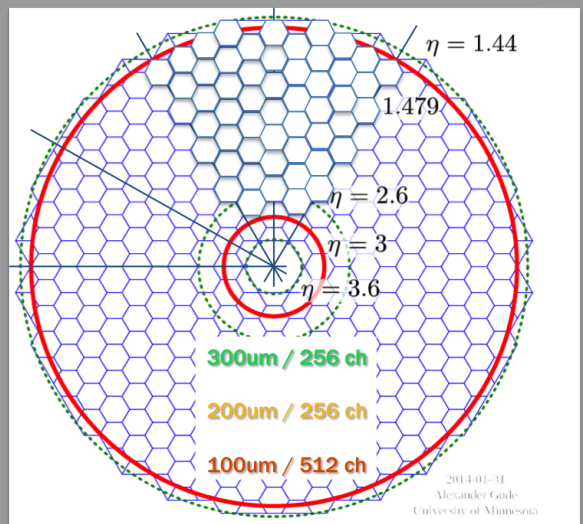
30 samplings of lead/copper – silicon
420 m^2 of silicon pad detectors
3.7 *Mchannels*

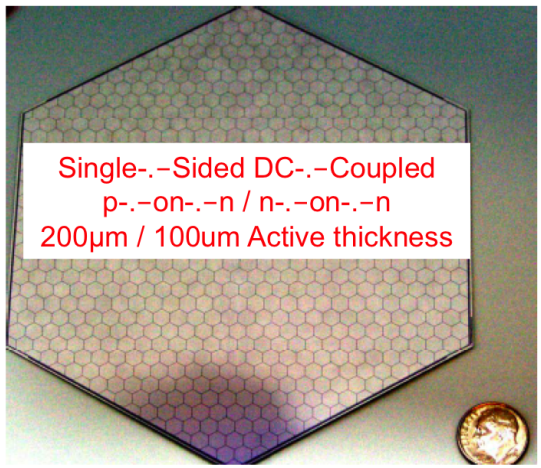
Front Hadronic Calorimeter

12 layers of brass – silicon
250 m^2 of silicon pad detector
1.4 *Mchannels*

Radiation levels

Up to 10^{16} $1MeV.n.cm^{-2}$ & several *MGy*

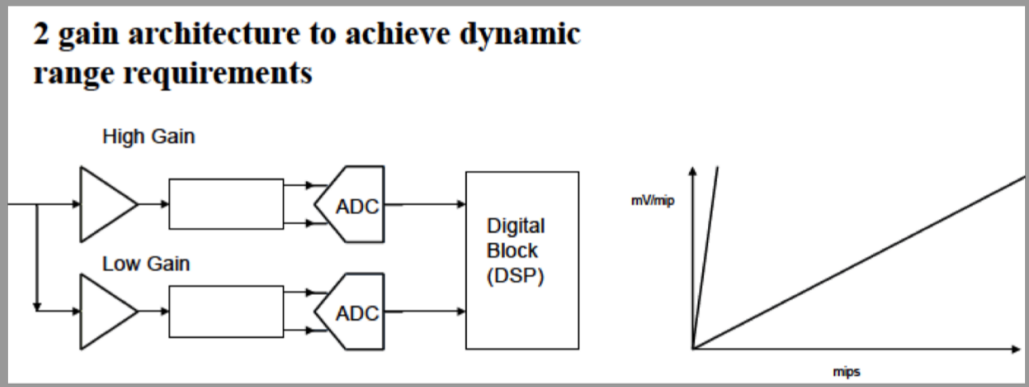


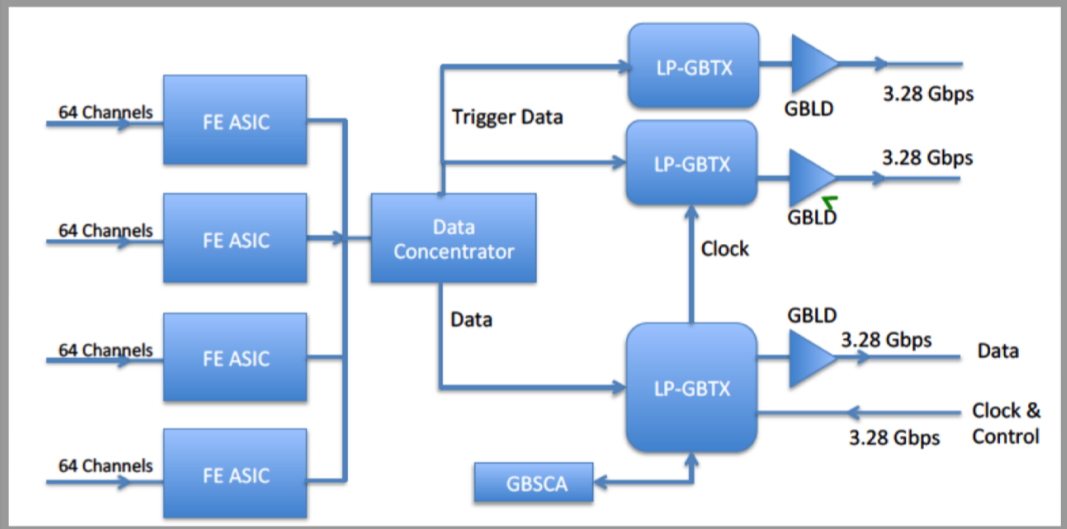


Electronics Challenges for HGC

Requirements

- 5.1 *Mchannels*
- Detector capacitance:
  - 50 – 100 *pF*
- Peaking time:
  - 15 – 20 *ns*
- Digitisation @ 40 *MHz*
  - Dynamic range: 1 to 10^4
  - Resolution 8 – 10 *bit*
- Trigger data @ 40 *MHz*
- Full readout @ L1 rate
- 15 *mW* per channel





~90000 electrical links & 15000 5 $Gb.s^{-1}$ optical links

Outline

Muon Detectors Upgrades

New chambers in the end-caps

- GEM chambers in CMS
- μmegas and sTGC in ATLAS (installation during LS2)

Electronics upgrade for some existing chambers

- Simplified front-end electronics of the CMS DT chambers
- Use of the ATLAS precision chambers in the trigger

Maintain existing front-end for some chambers?

- Because of access difficulties (time needed)
- Severe constraints on the overall system (latency and trigger rate)

Developments for the CMS GEM chambers

3 layers of GEM chambers in the end-caps

- Trigger improvement
- O(60 *kchannels*)

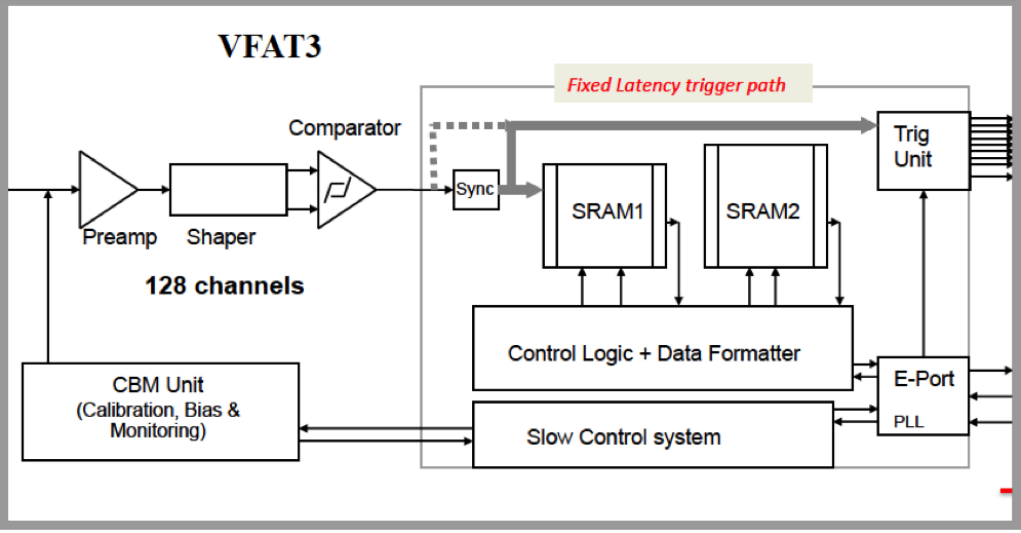
Front-end ASIC: VFAT3

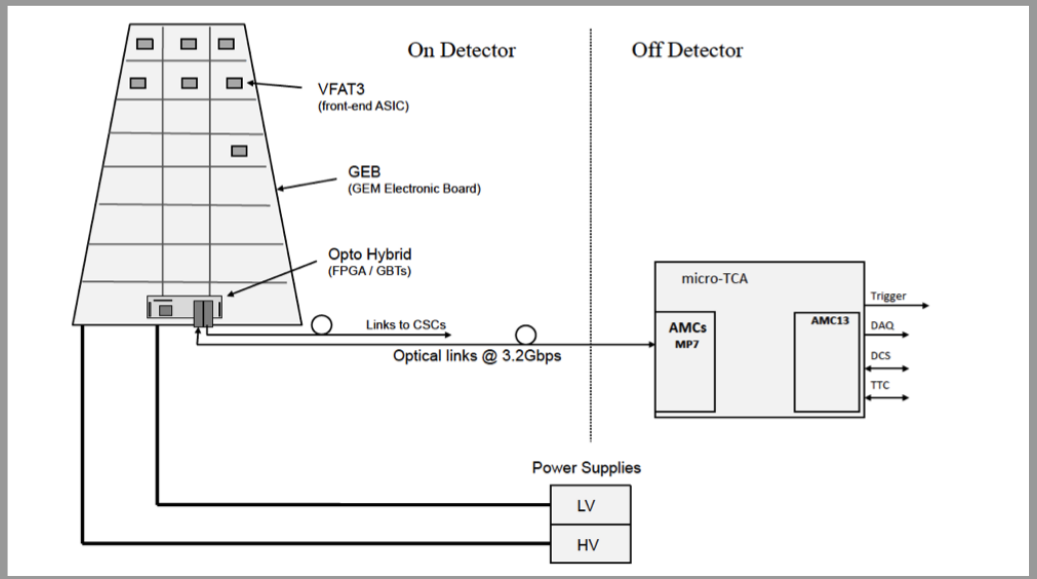
- 130 *nm* CMOS TSMC
- 128 channels
- Programmable shaping time: 25 – 400 *ns*
- Timing with CFD (no ToT)

Readout System

Based on the GBT

VFAT3 and Readout Simplified Block diagrams





Developments for the ATLAS New Small Wheels

Sandwiches of μmegas and sTGC in the end-cap NSW

- Trigger improvement to reduce high rate in the end-caps
- Both chambers participating in the trigger and readout
- O(2.3 *Mchannels*)

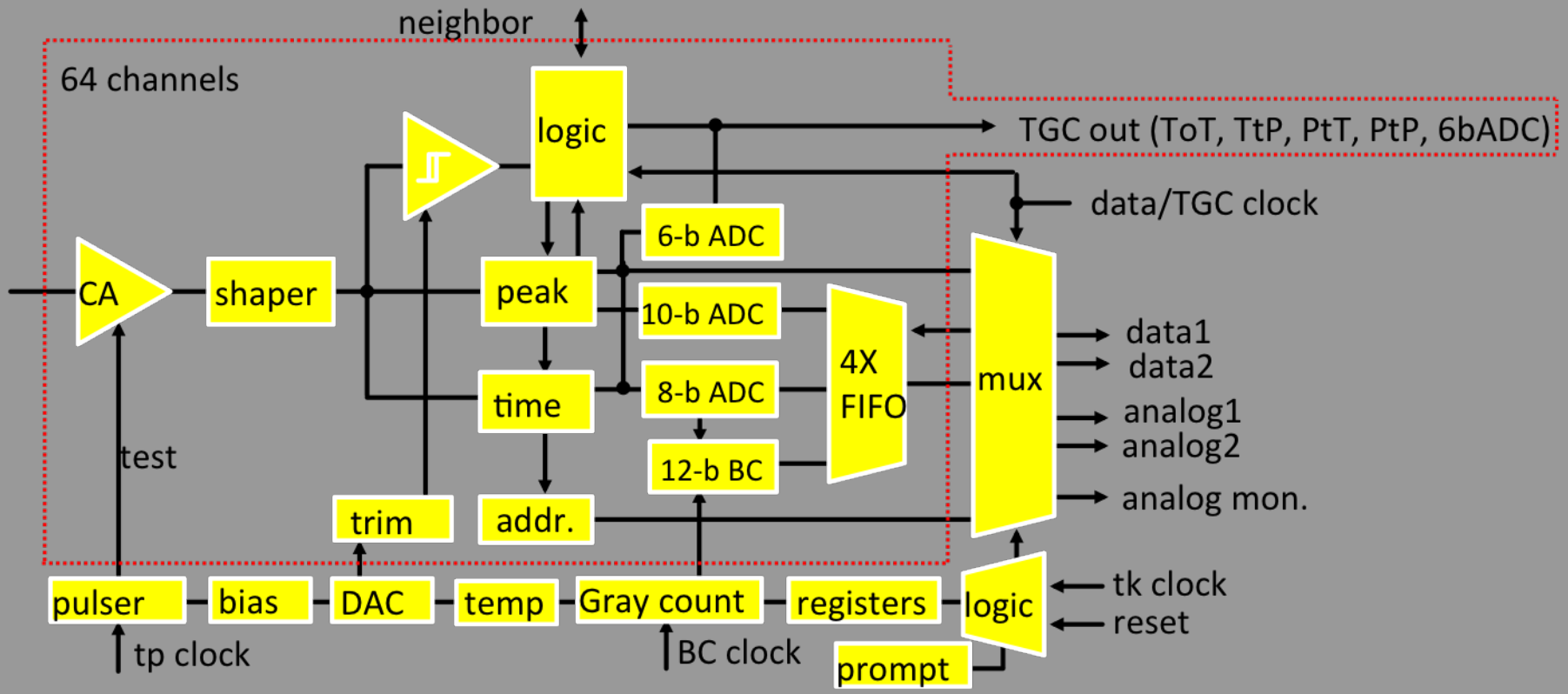
Front-end ASIC: VMM

- 64-channel 130 *nm* CMOS ASIC
- Q meas. up to 2 *pC* @ < 1 *fC rms*
- Time meas. 100 *ns* @ < 1 *ns rms*

Readout and Trigger Systems

Two others 130 *nm* CMOS ASICs

VMM Block Diagram



- coarse time counter: 12-bit Gray-code
- coarse threshold generator: 10-bit adjustable

Outline

Outline

IC Technologies

Used technologies

- So far most of the developments in 130 and 65 *nm* CMOS
- All developments in 130 *nm* using the IBM process
  - At the exception of VFAT3 (TSMC process to be used)

Expected schedule

Most of the ASICs to be produced until now and 2018

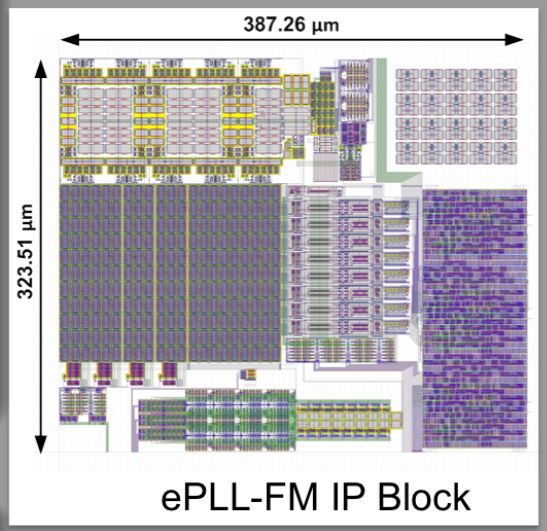
Some worries about the IBM process

- TSMC 130 *nm* being tested against radiation
- Moving from IBM to TSMC is not straight forward
- Strong interest in keeping the investment on IBM
- 6-month end of life warning

Sharing Designs

IP blocks

- RD53 started a full program of IP blocks development (in 65 *nm*)
- List of 30 required IPs defined
- Procedure for making IPs easily integrated into mixed signal design flow
- Repository



ePLL-FM IP Block

Should be extended to other technologies

- Already some blocks from the GBT available
  - e.g. SLVS I/Os, ePLL-CDR, ePLL-FM, ...

Radiation Hardness

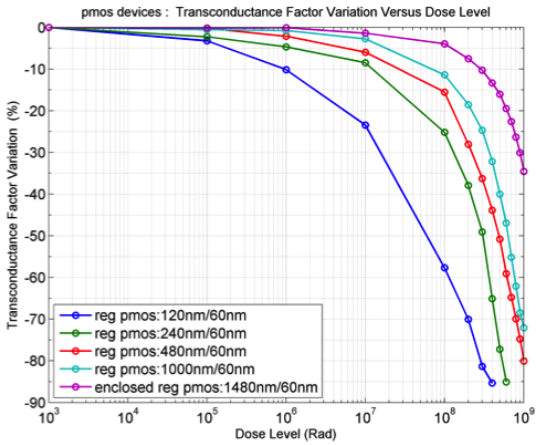
What seems OK

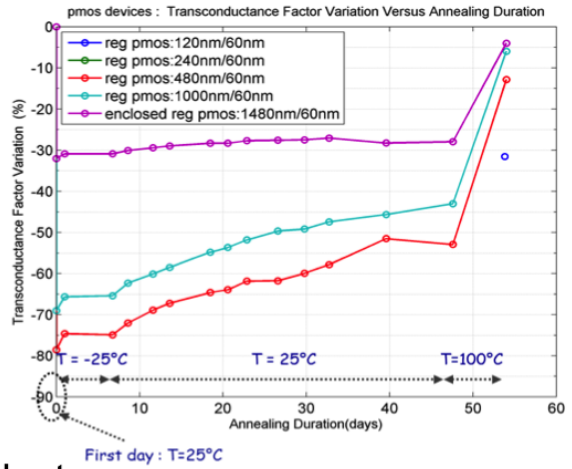
- IBM 130 *nm* and TSMC 65 *nm* radiation hard enough for outer pixel layers and outer trackers
- TSMC 130 *nm* to be qualified (see MUG session)

What seems not OK

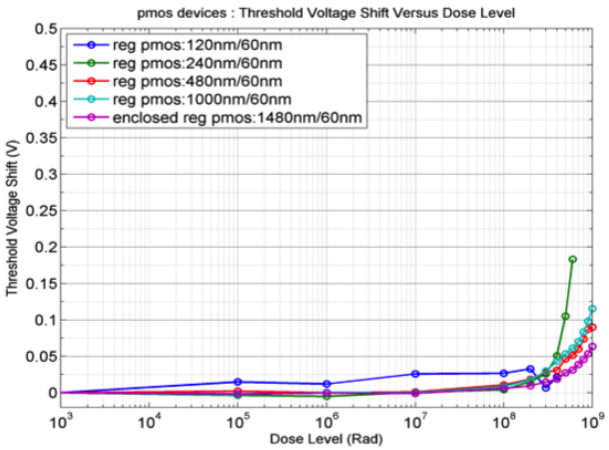
- Some problems at very high dose for the 65 *nm*
- Severe issue for the inner pixel layers
  - Might require to come back to a replacement scenario for these layers
  - As it was foreseen for the current inner pixel layers

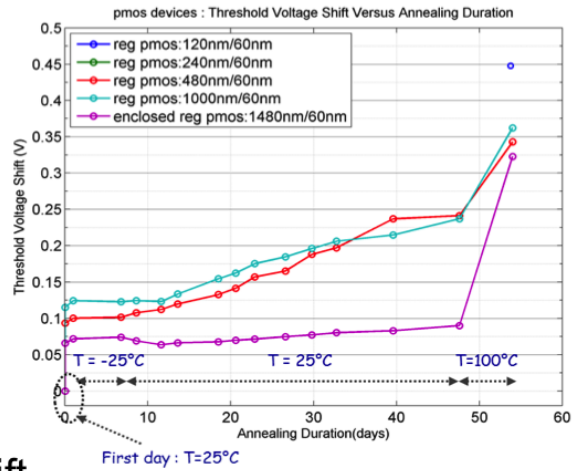
Radiation Effect on a 65 *nm* PMOS Transistor





Transconductance





Vt shift

Outline

On-going Developments

Serialisers-Deserialisers and Optical Links

- Several developments mentionned
- Common developments
  - GBT chipset and Versatile Link

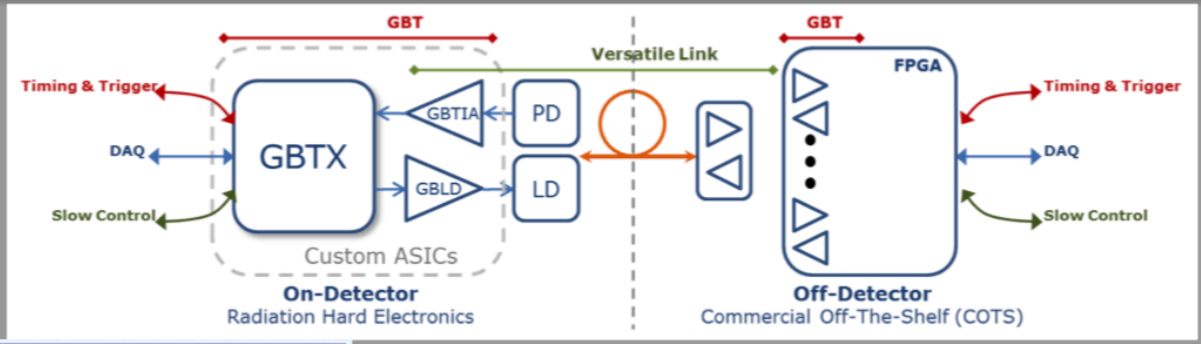
Status of the GBT chipset

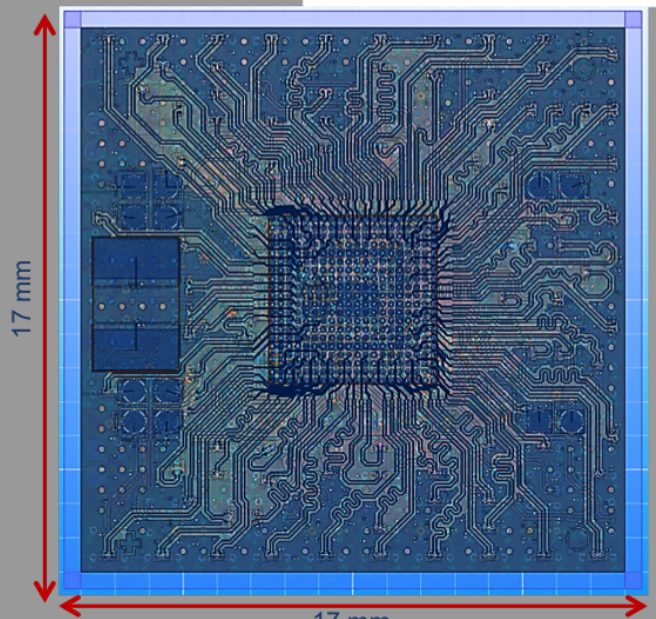
- GBTX, GBT-SCA, GBLD, GBTIA
  - 4.8 $Gb.s^{-1}$, 130 nm
- Engineering run launched
- Full production Spring 2015

Status of the Versatile Link

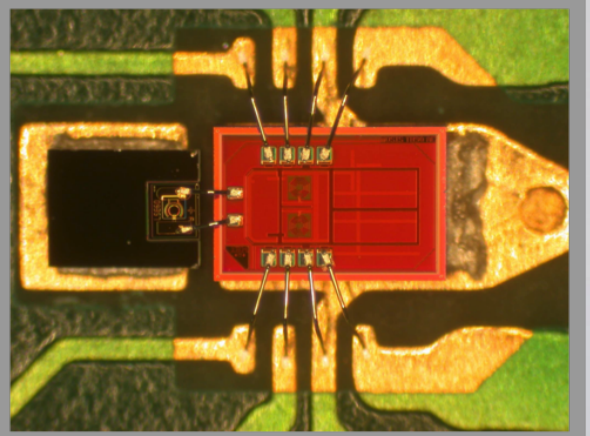
- Transceiver or dual emitter (VTRX and VTTX)
  - 5 $Gb.s^{-1}$
  - Multi- or Single-mode
- Full production Spring 2015

GBT chipset and Versatile Link

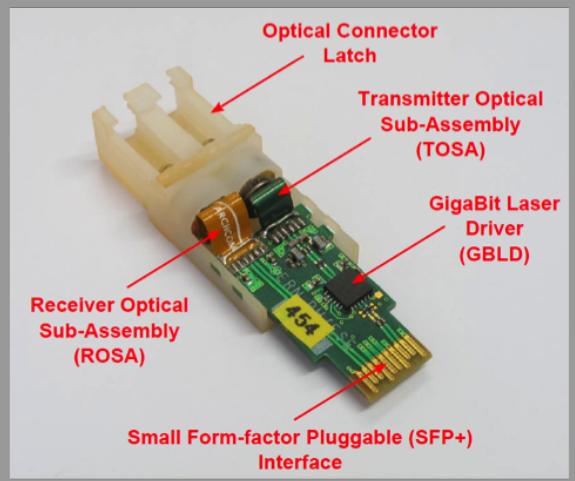




GBTX



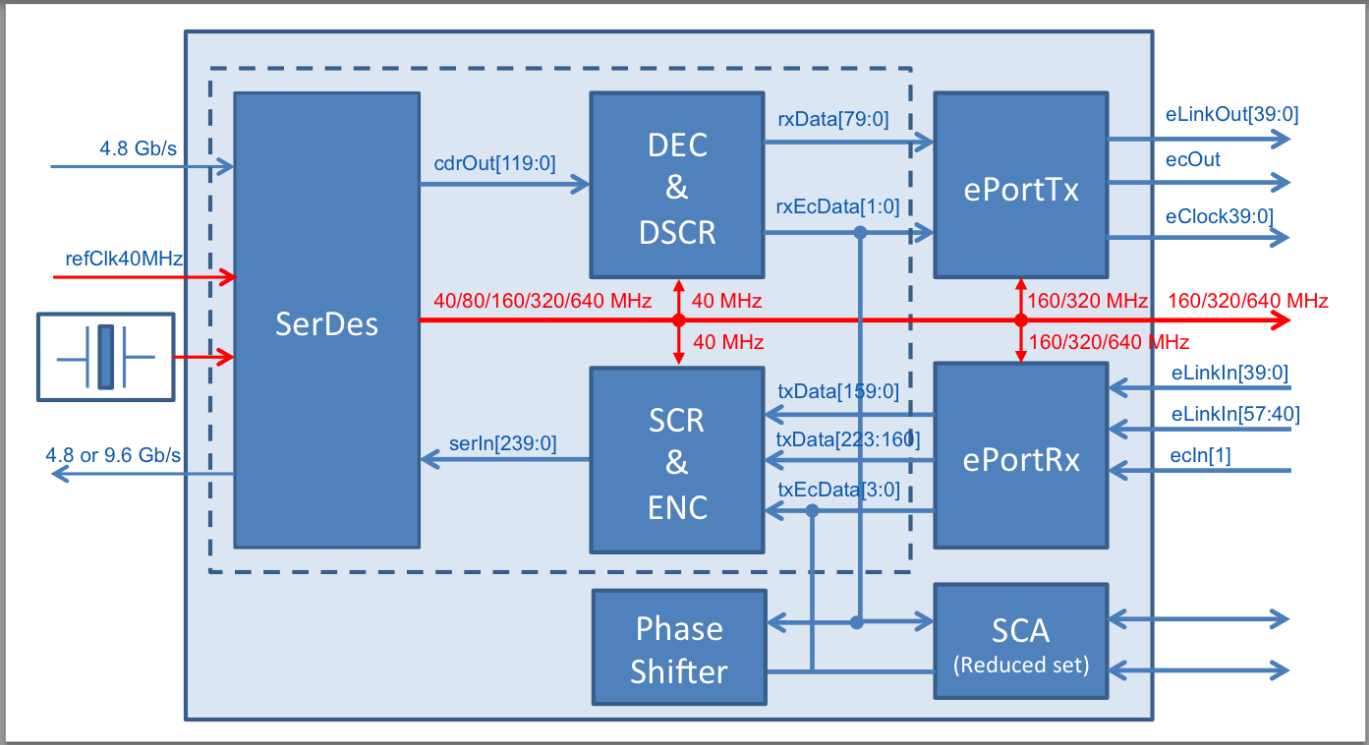
GBTIA



VTRX

Smaller, less power hungry or faster version needed for HL-LHC

The Low Power GBT: lpGBT



- Low power and small footprint
  - 450 *mW* @ 4.8 $Gb.s^{-1}$
- 4.8 $Gb.s^{-1}$ for down links
- 4.8 $Gb.s^{-1}$ or 9.6 $Gb.s^{-1}$ for up links
- e-Links up to 640 $Mb.s^{-1}$
- Single-ended or differential
- Subset of the GBT-SCA
- 65 *nm* CMOS

Versatile Link for HL-LHC: the VL+ Project

Small form factor, high speed needed

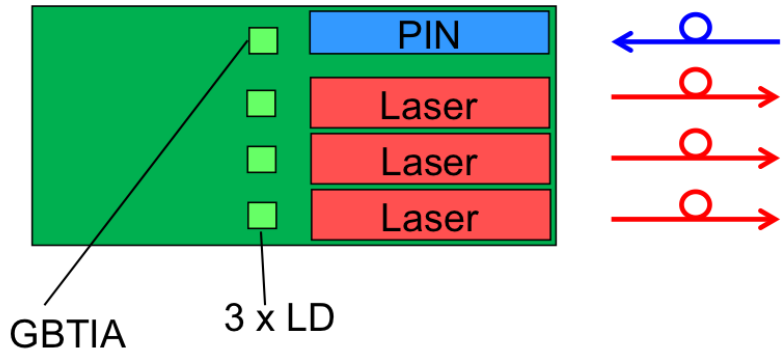
- 5/10 $Gb.s^{-1}$ up/down links
- CMS tracker modules, ATLAS EoS
- High density links for calorimeters

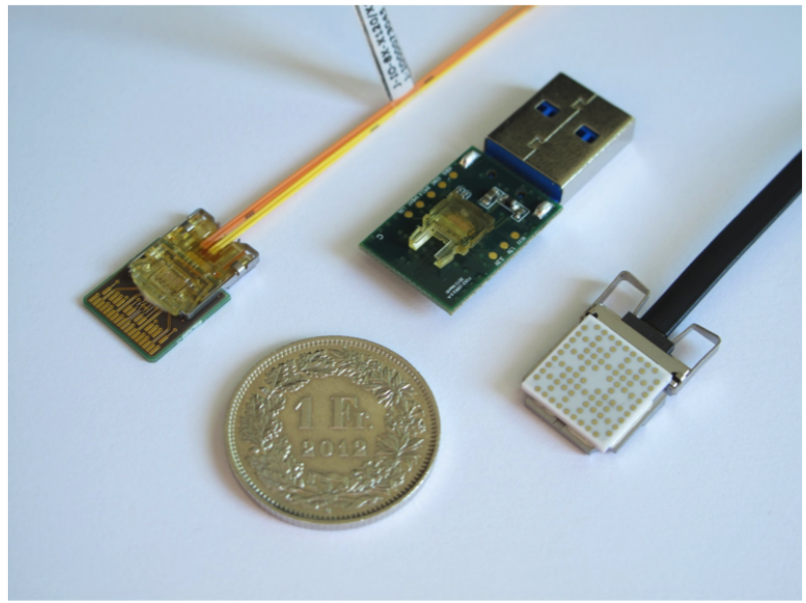
High versatility

- Number of up/down links

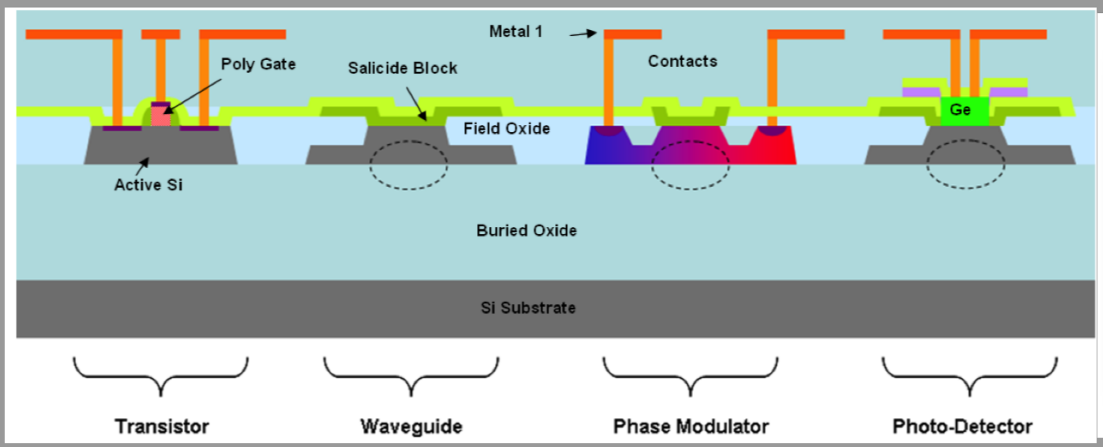
On-going work

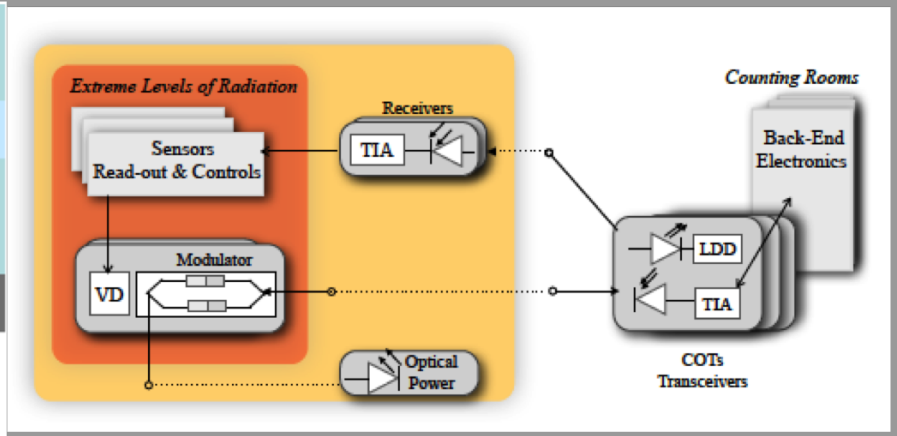
- 10 $Gb.s^{-1}$ tiny single/quad LD
- Package, fibres, connectors
- Feasibility study until fall 2015





Silicon Photonics: a Dream?





- Si is an excellent optical material
- Could build a photonic circuit in a CMOS Si-wafer
- Huge potential gain
  - Power and integration

- Commercial devices tested
- Collaborations with industrial partners
- Some building blocks under test
- Packaging is challenging
- Assess radiation hardness first!

Outline

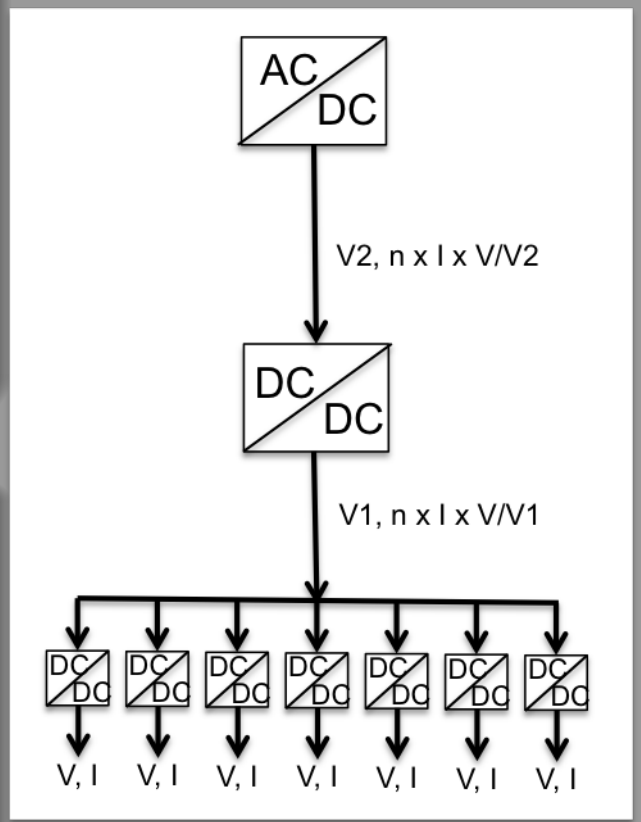
Common Power Scheme?

Possible common power structure

- Several stages of converters
  - POL DC-DC and/or Linear VR at the load
- Specifications needed
  - Environmental conditions (radiation)
  - Input/Output voltages and power
  - Common devices possible

Tracker powering

- DC-DC converters
  - Radiation and magnetic tolerant
- Serial powering scheme
  - Successfully tested on an ATLAS stave
  - Only viable solution for the pixel detectors?



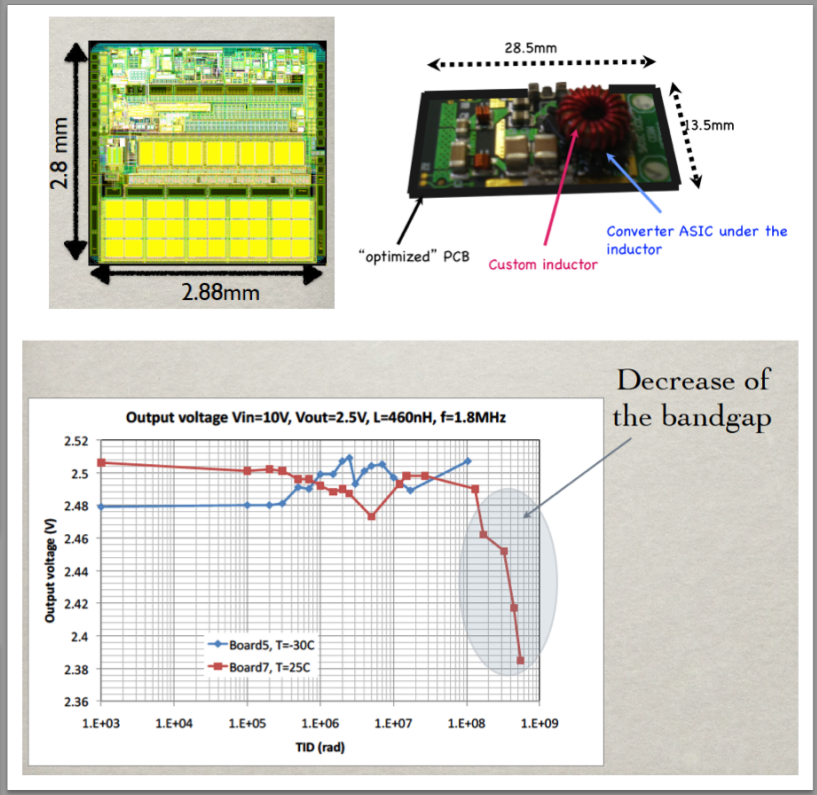
Radiation and Magnetic Field Tolerant POL DC-DC

Specific development for the trackers

- Started in 2008, now in production
  - ASIC (.35 μm) and complete module
  - 5 – 12 V Vin, 0.9 – 5 V Vout, 4 A
  - >2 MGy and 8 10^{14} $1MeV.n.cm^{-2}$
- Some limitations for inner layers of trackers @ HL-LHC

Further developments

- New ASIC needed
- Evaluate GaN power switches



Outline

Outline

Where were we 11 Years before LHC Start?

Date of LHC start

- Moving target however two dates emerge
  - Fall 2006 and Fall 2008
- Information from LERB, LECC Workshops
  - Lisbon 1995 or London 1997

We were far away from the final systems

- 0.25 μm CMOS presented in 1998
- Optical links using modulators or LEDs
- Massive usage of FPGA barely emerging

We should keep our eyes opened

- We might be lucky again...

Summary

- HL-LHC imposes strong constraints on the readout electronics
  - High radiation levels
  - Large amount of data to be handled
- A lot of developments are on-going
  - ASIC developments
  - Trigger architecture
- Common developments on specific topics
  - Pixel electronics
  - "Common projects" (links, DC-DC converters)
- Still space for more common developments
  - IP blocks
  - Common power blocks
- 11 years to go before HL-LHC starts
  - We should keep our eyes opened...

Sources and Acknowledgements

Sources

ACES 2014: *http://indico.cern.ch/e/ACES2014*
ECFA workshop on HL-LHC: *https://indico.cern.ch/event/252045/*
ATLAS and CMS LoI, TP, etc.
TWEPP: *http://twepp-workshops.web.cern.ch/TWEPP-Workshops/*

Special thanks to

Paul Aspell, Philippe Bloch, Jorgen Christiansen, Francesco Lanni, François Vasey